

# Fundamentals of microelectronics processes

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# Several aspects of processing

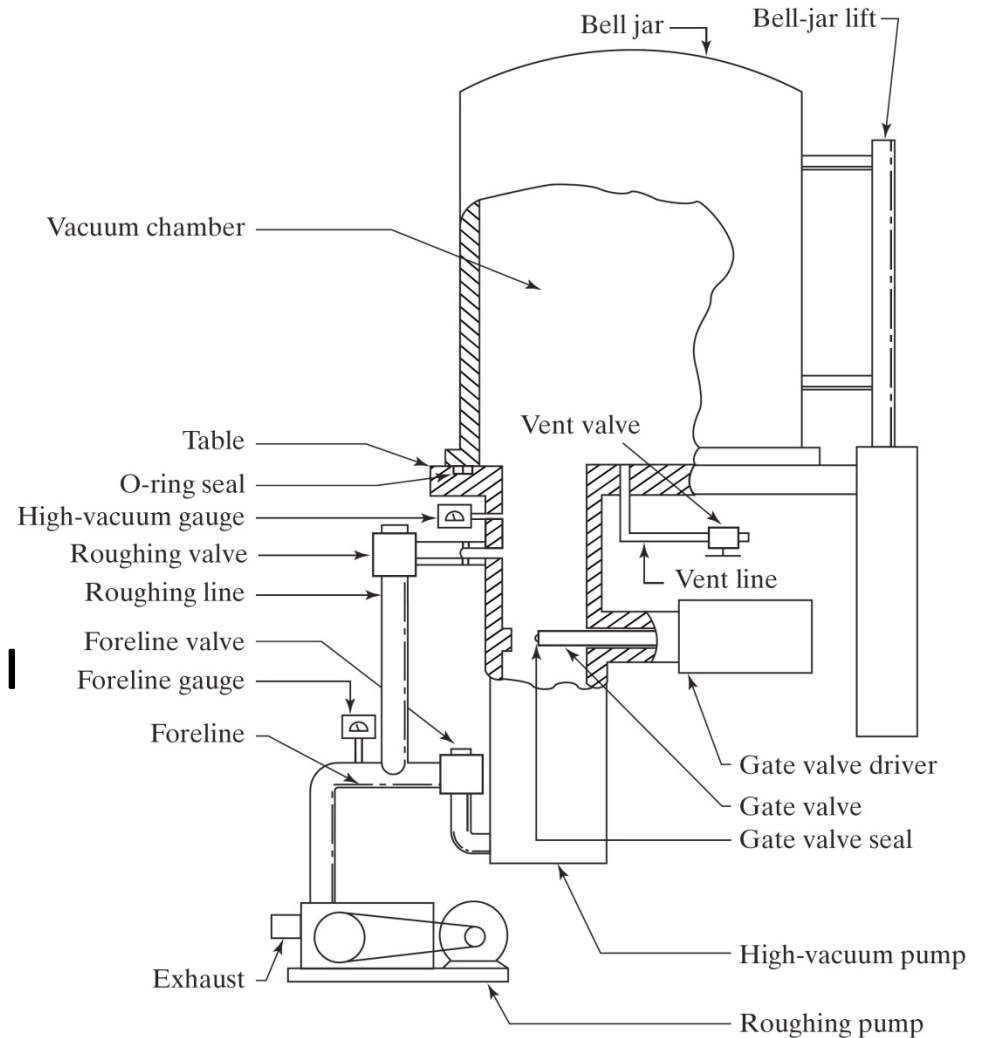
- Chemistry and physics of the process
- Process variables and figure of merits
- Machine operation procedure - safety
- Principle of machine operation and machine parts
  - Vendors and pricing of machine, parts, supplies
- Electronic and mechanical subsystems of machine
- Supplies for the process
- Safety precautions and potential hazards
- Process behavior with materials and wafers
  - Rate
  - Uniformity
  - Repeatability
  - Temperature or chemical stability
  - Peculiarities (how does the process work differently after so and so worked on it before you ☺).
- Jargons

# Metalization

- Sputtering
- Evaporation
  - Electron beam evaporation
  - Thermal evaporation
- Electroplating
- Electroless plating

# General Vacuum Equipment Parts

- Deposition sources
- Evaporation chamber
- Vacuum pumps
  - Roughing pumps
  - High vacuum pumps
- Deposition rate monitor



# Vacuum Jargon

- 1 ATM=760 torr
- 1 pascal = 1 N/m<sup>2</sup>
- 1 torr= 133.322 Pascals

Pressure Units

	pascal (Pa)	bar (bar)	technical atmosphere (at)	atmosphere (atm)	torr (Torr)	pound-force per square inch (psi)
1 Pa	≡ 1 N/m <sup>2</sup>	10 <sup>-5</sup>	1.0197×10 <sup>-5</sup>	9.8692×10 <sup>-6</sup>	7.5006×10 <sup>-3</sup>	145.04×10 <sup>-6</sup>
1 bar	100,000	≡ 10 <sup>6</sup> dyn/cm <sup>2</sup>	1.0197	0.98692	750.06	14.5037744
1 at	98,066.5	0.980665	≡ 1 kgf/cm <sup>2</sup>	0.96784	735.56	14.223
1 atm	101,325	1.01325	1.0332	≡ 1 atm	760	14.696
1 torr	133.322	1.3332×10 <sup>-3</sup>	1.3595×10 <sup>-3</sup>	1.3158×10 <sup>-3</sup>	≡ 1 Torr; ≈ 1 mmHg	19.337×10 <sup>-3</sup>
1 psi	6,894.76	68.948×10 <sup>-3</sup>	70.307×10 <sup>-3</sup>	68.046×10 <sup>-3</sup>	51.715	≡ 1 lbf/in <sup>2</sup>



This is a dual e-beam/thermal evaporator for the deposition of Au, Ag, Cu, Ni, Cr, Al, Ti, Fe, Co, W, Gd, Nb, Ta, permalloy, Si, and  $\text{Al}_2\text{O}_3$ .  
6-pocket electron gun  
two electrodes for thermal sources  
wafers from 2" to 6"  
capacity: 4 wafers  
cryopumped with a base vacuum of  $5\text{E-}8\text{T}$   
uniformity shield yielding thickness uniformity of 4 % over 4" wafers.

filaments



Basket  
heater



boxes



boats



rods



# Vacuum pumps

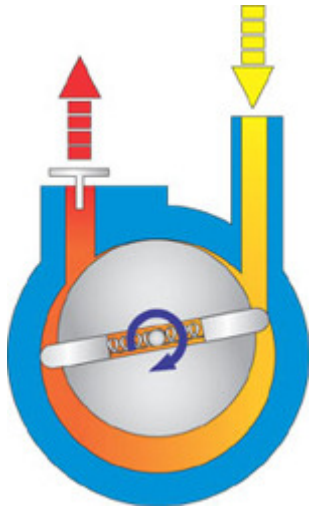
- **Coarse Vacuum** — 760–1 Torr
- **Rough Vacuum** — 760– $10^{-3}$  Torr
- **High Vacuum** —  $10^{-4}$ – $10^{-8}$  Torr
- **Ultra High Vacuum** —  $10^{-9}$ – $10^{-12}$  Torr

How many particles are there?

.



# Pump Principles

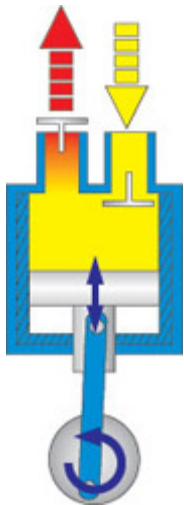


## Rotary Vane Pump

**Vacuum Level:** Coarse Vacuum or Rough Vacuum (design dependent)

**Gas Removal Method:** Gas Transfer

**Pump Design:** Oil-Sealed (wet)



## Piston pump

**Vacuum Level:** Rough Vacuum

**Gas Removal Method:** Gas Transfer

**Pump Design:** Dry

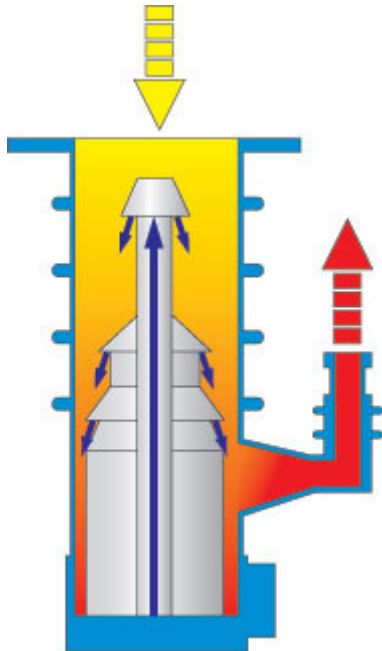
Kinney-tuthill  
Rotary piston pump



Edwards  
EM series rotary pump



# Pumping Principles

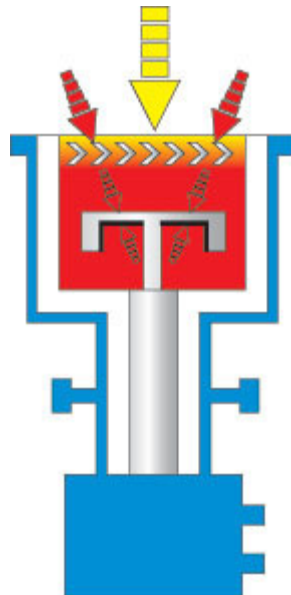


Diffusion pump  
 $10^{-4}$ - $10^{-7}$  torr

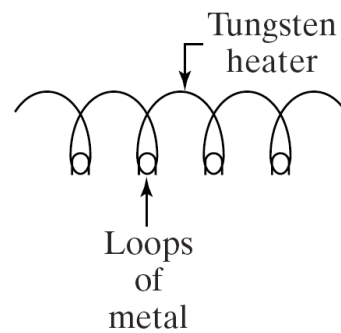


Varian DPD series  
Diffusion pump

Cryogenic pumps

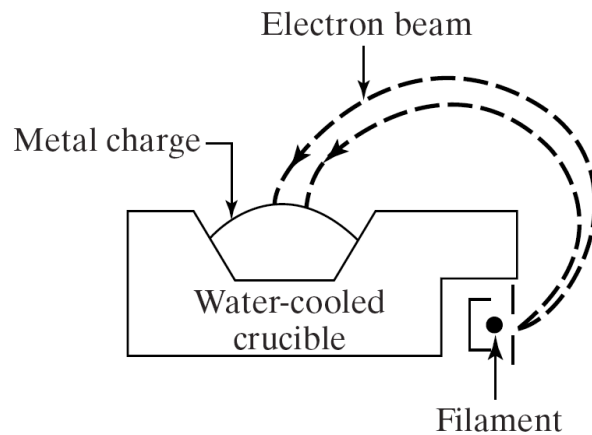


# Evaporation Filament & Electron Beam



(a)

(a) Filament Evaporation with Loops of Wire Hanging from a Heated Filament



(b)

(b) Electron Beam is Focused on Metal Charge by a Magnetic Field

# Evaporation rate

# Mean free path of particles

.

# Evaporation

## Shadowing and Step Coverage

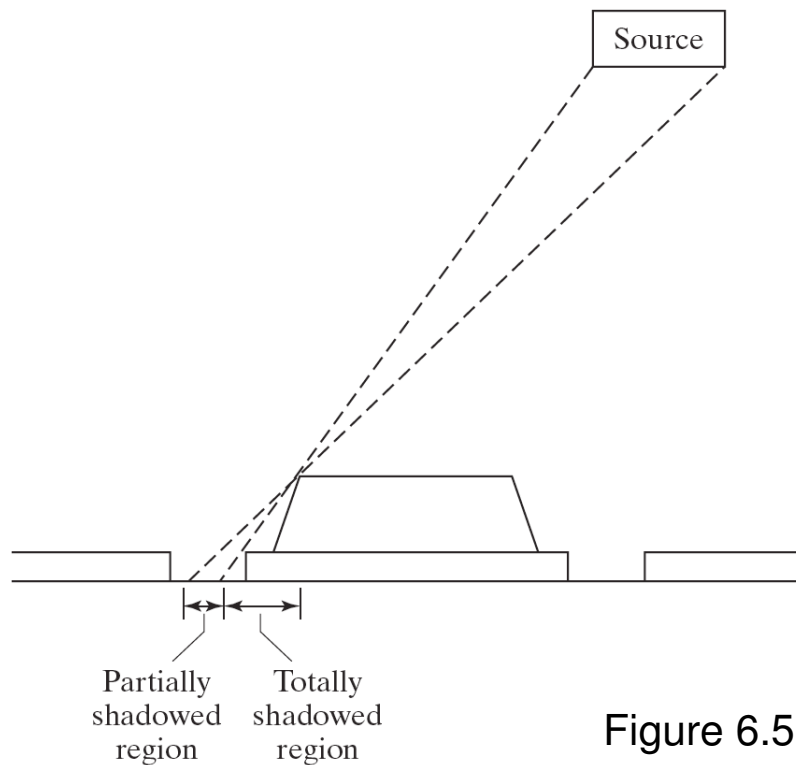


Figure 6.5

- Shadowing and Step Coverage Problems Can Occur in Low Pressure Vacuum Deposition in which the Mean Free Path is Large

# Types of coverage

- Conformal coverage
- Non conformal coverage

# Film Deposition

## Sputtering

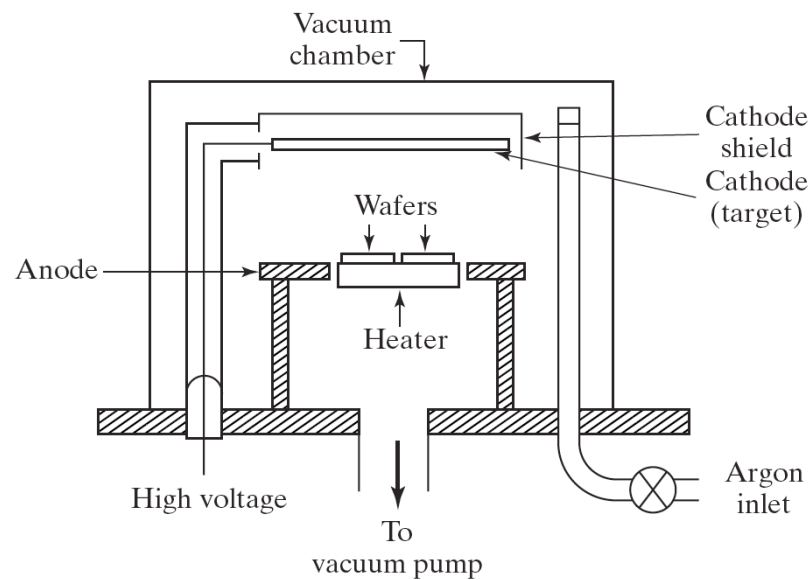


Figure 6.6

A dc sputtering system in which the target material acts as the cathode of a diode and the wafers are mounted on the system anode.

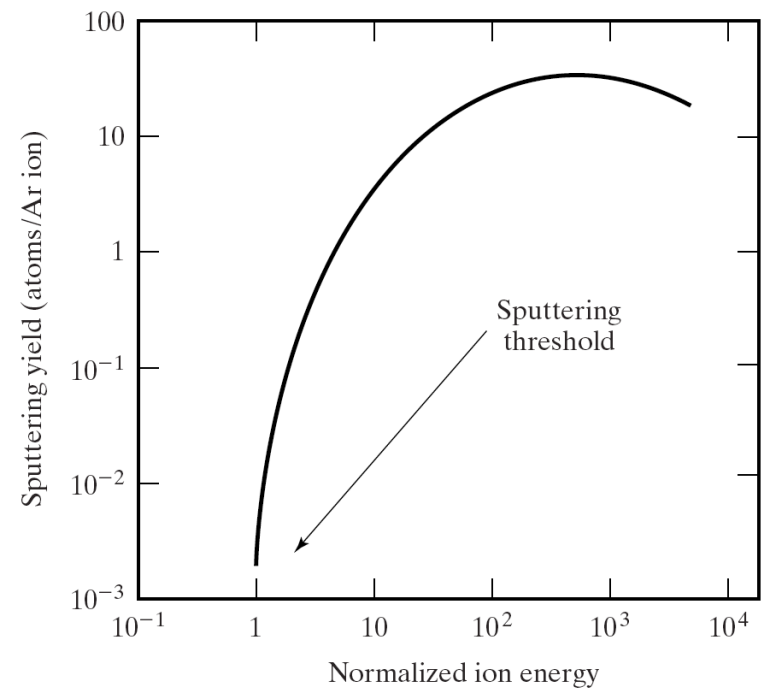
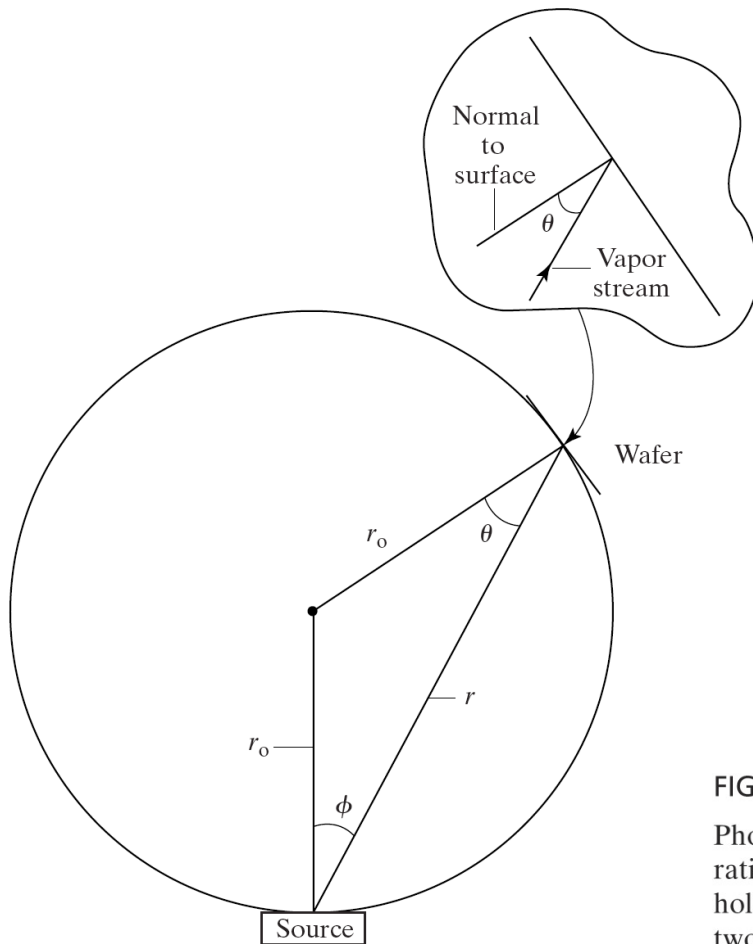


Figure 6.7

Sputtering yield increases rapidly as ion energy is increased above the sputtering threshold (argon)



# Evaporation Electron Beam



Growth Rate

$$G = \frac{m}{\pi \rho r^2} \cos \phi \cos \theta$$

$$\cos \phi = \cos \theta = \frac{r}{2r_o}$$

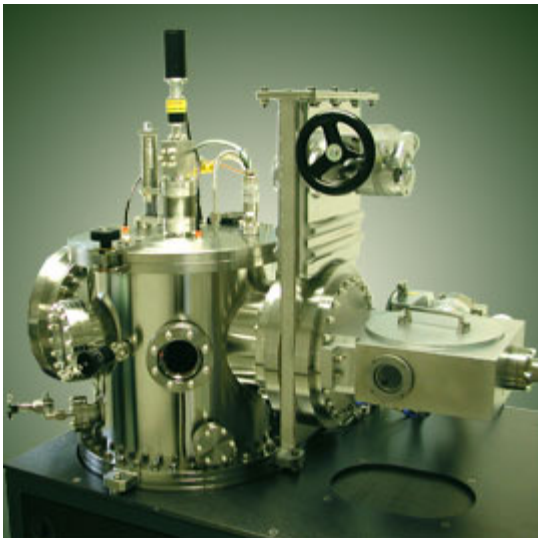
$$G = \frac{m}{4 \pi \rho r_o^2}$$

FIGURE 6.4

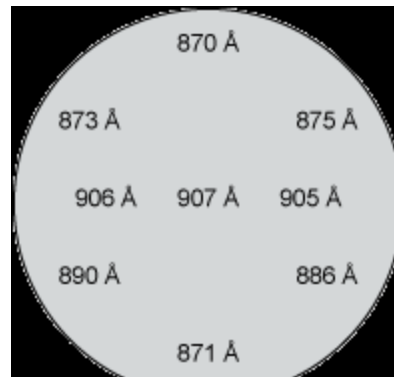
Photograph of a laboratory E-beam evaporation system with a planetary substrate holder which rotates simultaneously around two axes.

# Sputtering

- DC vs. RF
- Metal
- Insulator
- Alloy
- Gas mixture



AJA Orion 8



Deposition of SiO<sub>2</sub> on 100mm diameter Si wafer at 150 Watts, 3mTorr, 5.5" working distance. Uniformity is  $\pm 2.08\%$

# Typical system components



Substrate heater



Vacuum pumps



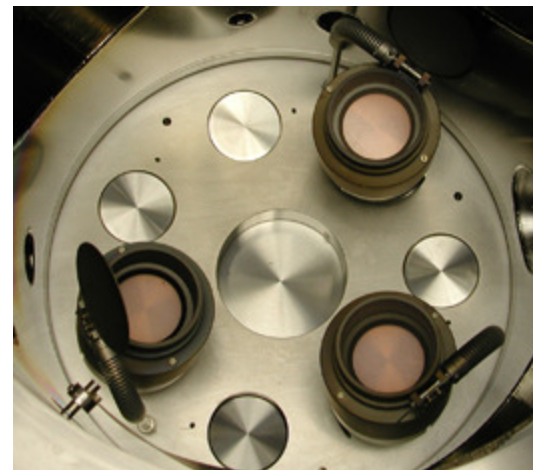
Power distribution modules



Computer control



Targets



Cluster

# Pros and Cons

- Thermal evaporator
  - High temperature
  - Rapid deposition
  - Equipment low cost
- Sputtering
  - Low temperature
  - Better step coverage
  - Equipment expensive

# Introduction to Microelectronic Fabrication

by

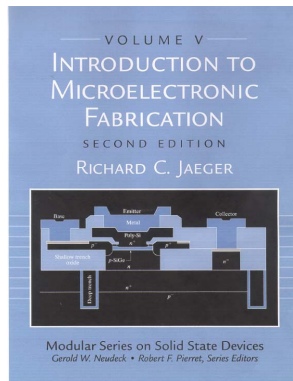
Richard C. Jaeger

Distinguished University Professor

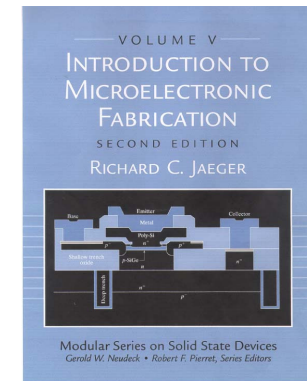
ECE Department

Auburn University

## Chapter 2 Lithography

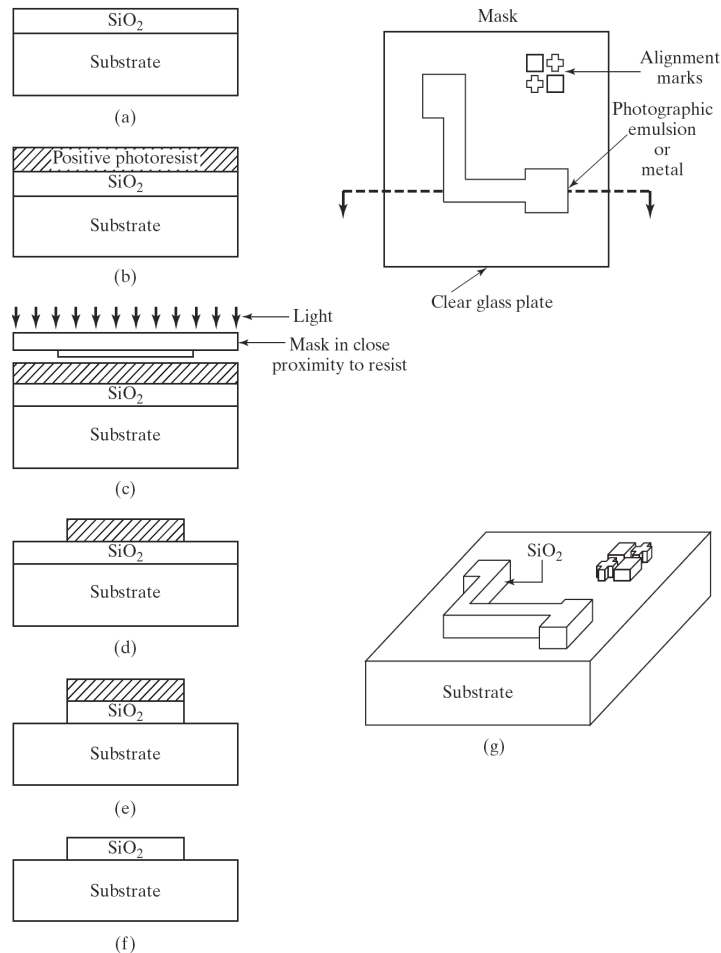


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Introduction to Microelectronic Fabrication,  
Second Edition by Richard C. Jaeger. ISBN0-201-  
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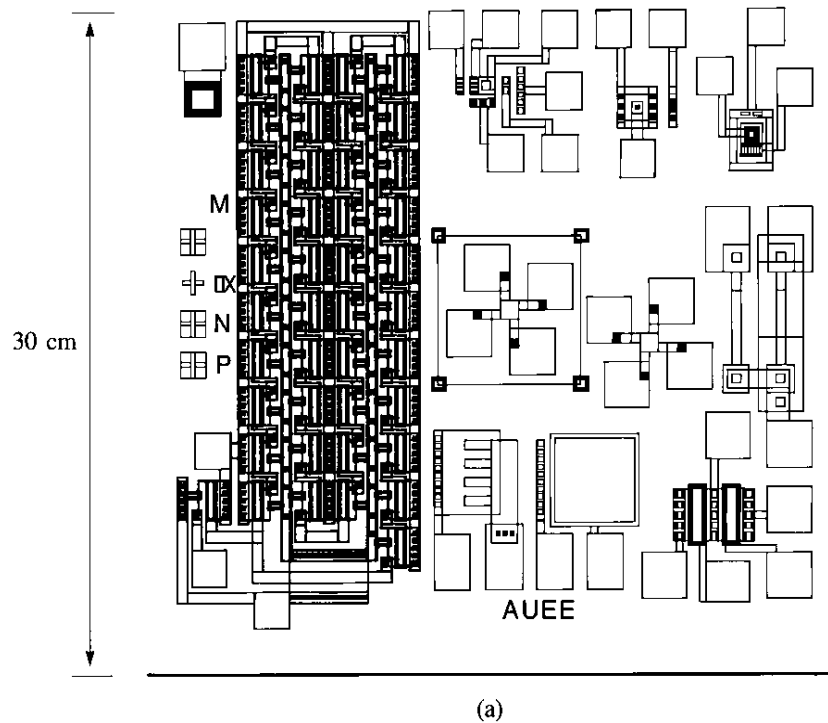
# Photolithographic Process



- (a) Substrate covered with silicon dioxide barrier layer
- (b) Positive photoresist applied to wafer surface
- (c) Mask in close proximity to surface
- (d) Substrate following resist exposure and development
- (e) Substrate after etching of oxide layer
- (f) Oxide barrier on surface after resist removal
- (g) View of substrate with silicon dioxide pattern on the surface

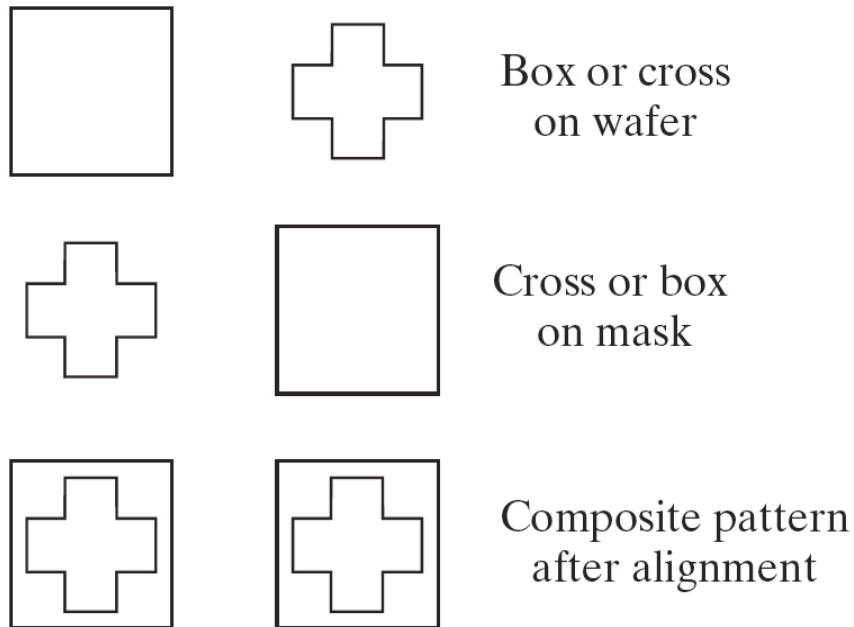
# Photomasks

## CAD Layout



- Composite drawing of the masks for a simple integrated circuit using a four-mask process
- Drawn with computer layout system
- Complex state-of-the-art CMOS processes may use 25 masks or more

# Mask Alignment



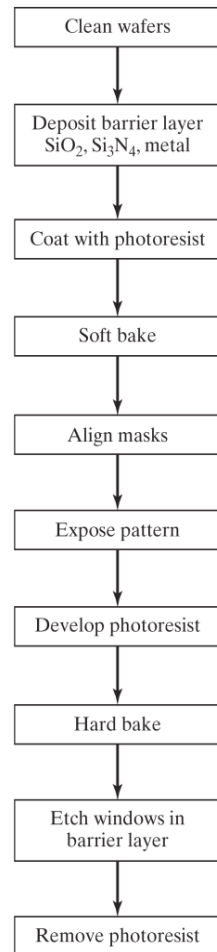
- Each mask must be carefully aligned to the previous levels
- Some form of alignment marks are used
- Automated alignment and exposure in production lines



# ITRS Lithography Projections

Table 2.5 -- ITRS Lithography Projections						
Year	2001	2003	2005	2008	2011	2014
Dense Line Half-Pitch (nm)	150	120	100	70	50	35
Worst Case Alignment Tolerance Mean + 3 $\sigma$ (nm)	52	42	35	25	20	15
Minimum Feature Size F (nm) Microprocessor Gate Width	100	80	65	45	30	20
Critical Dimension Control (nm) Mean + 3 $\sigma$ - Post Etching	9	8	6	4	3	2
Equivalent Oxide Thickness (nm)	1.5 - 1.9	1.5 - 1.9	1.0 - 1.5	0.8 - 1.2	0.6 - 0.8	0.5 - 0.6
Lithography Technology Options	248 nm DUV	248 nm + PSM 193 nm DUV	193 nm + PSM 157 nm E-beam projection Proximity x-ray Ion Projection	157 nm +PSM E-beam projection E-beam direct write EUV Ion Projection Proximity x-ray	EUV E-beam projection E-beam direct write Ion Projection	EUV E-beam projection E-beam direct write Ion Projection Innovation
DUV - deep ultraviolet; EUV - extreme ultraviolet; PSM - phase shift mask;						

# Photolithographic Process



- Each mask step requires many individual process steps
- Number of masks is a common measure of overall process complexity

# Wafer Cleaning

- Wafers must be cleaned of chemical and particulate contamination before photo processing
- Example of “RCA” cleaning procedure in table below

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TABLE 2.2 Silicon Wafer Cleaning Procedure<sup>[4,5]</sup>

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**A. Solvent Removal**

1. Immerse in boiling trichloroethylene (TCE) for 3 min.
2. Immerse in boiling acetone for 3 min.
3. Immerse in boiling methyl alcohol for 3 min.
4. Wash in DI water for 3 min.

**B. Removal of Residual Organic/Ionic Contamination**

1. Immerse in a (5:1:1) solution of  $\text{H}_2\text{O}$ – $\text{NH}_4\text{OH}$ – $\text{H}_2\text{O}_2$ ; heat solution to 75–80 °C and hold for 10 min.
2. Quench the solution under running DI water for 1 min.
3. Wash in DI water for 5 min.

**C. Hydrous Oxide Removal**

1. Immerse in a (1:50) solution of  $\text{HF}$ – $\text{H}_2\text{O}$  for 15 sec.
2. Wash in running DI water with agitation for 30 sec.

**D. Heavy Metal Clean**

1. Immerse in a (6:1:1) solution of  $\text{H}_2\text{O}$ – $\text{HCl}$ – $\text{H}_2\text{O}_2$  for 10 min at a temperature of 75–80 °C.
  2. Quench the solution under running DI water for 1 min.
  3. Wash in running DI water for 20 min.
-

# Piranha Cleaning

- Clean organic residue
- Mix 4:1  $\text{H}_2\text{SO}_4$  (pure or 98%) and  $\text{H}_2\text{O}_2$ 
  - Solution will heat up
- Heat up to  $100^\circ\text{C}$ 
  - Fresh piranha solution should bubble
- Dip wafer using Teflon holders or quartz holders
- Hold for a certain time, rinse.



# Photoresist spin coating

- Mechanism
- Thickness control
- Defects (edge beading)

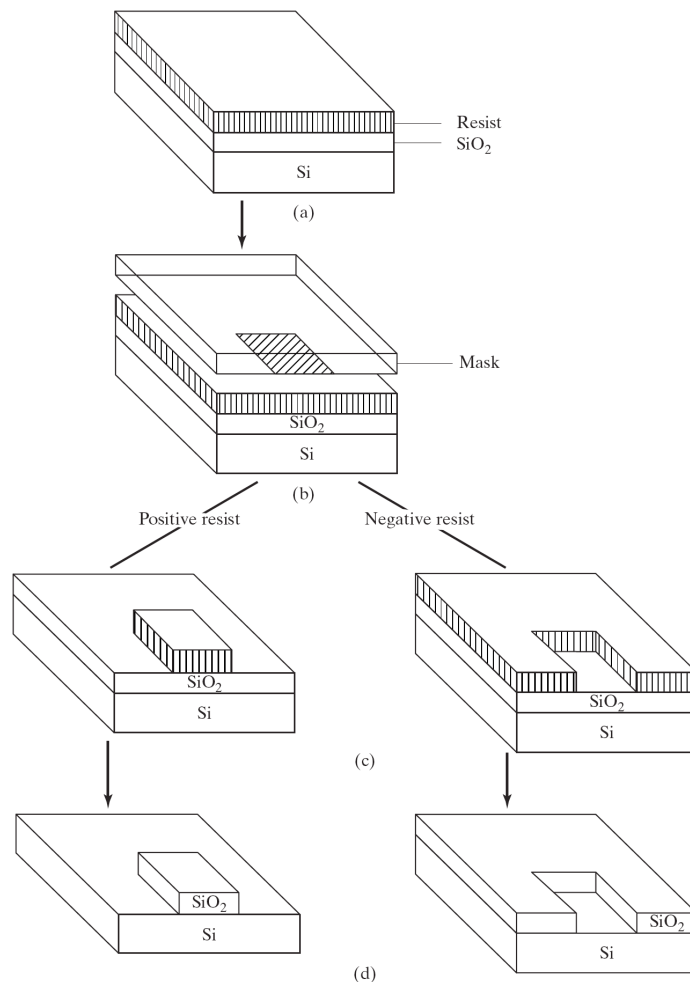
# Photoresist Deposition

## Automated Production Systems



- Rite Track 88e wafer processing system (Courtesy of Rite Track Services, Inc.)

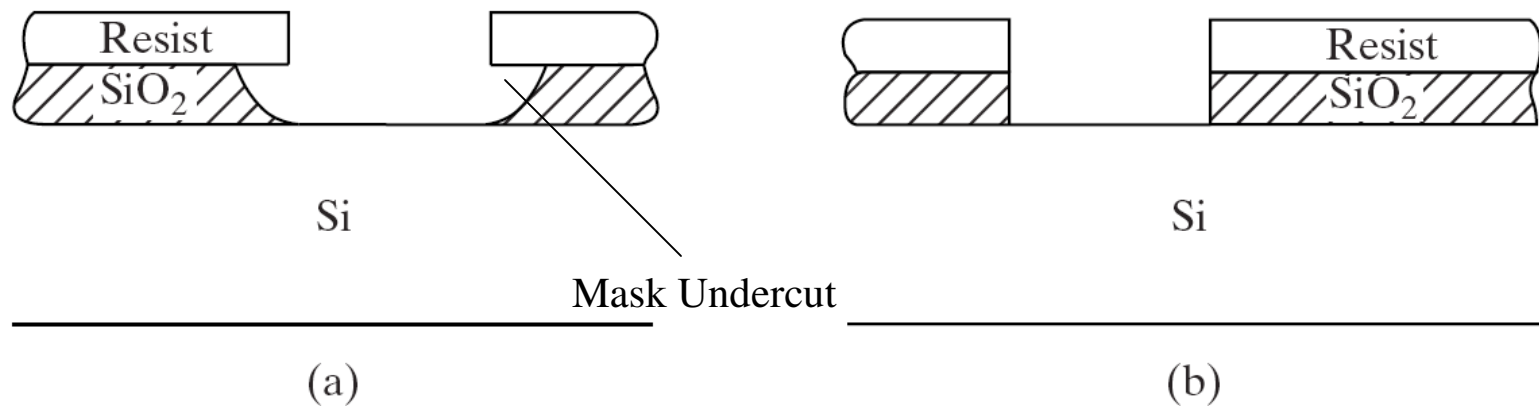
# Resists for Lithography



- Resists
  - Positive
  - Negative
- Exposure Sources
  - Light
  - Electron beams
  - Xray sensitive

# Oxide Etching Profiles

- (a) Isotropic etching - wet chemistry - mask undercutting
- (b) Anisotropic etching - dry etching in plasma or reactive ion etching system

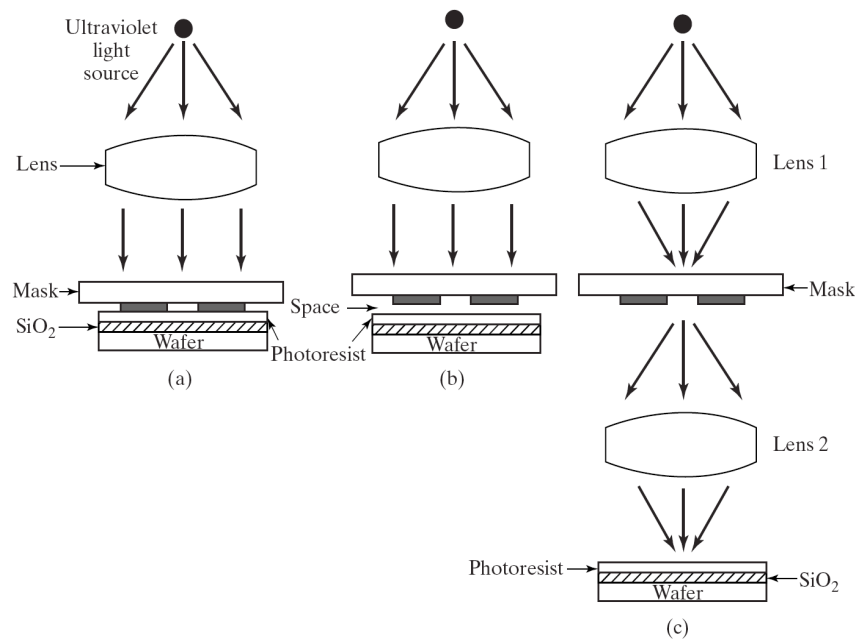




# Printing Techniques

- Non-contact exposure
  - Light path management
  - Reduction ratio possible
  - Stepper
  - Large mask
- Contact exposure
  - Minimize diffraction
  - 1:1
  - Contact aligner
  - Contamination prone

# Printing Techniques

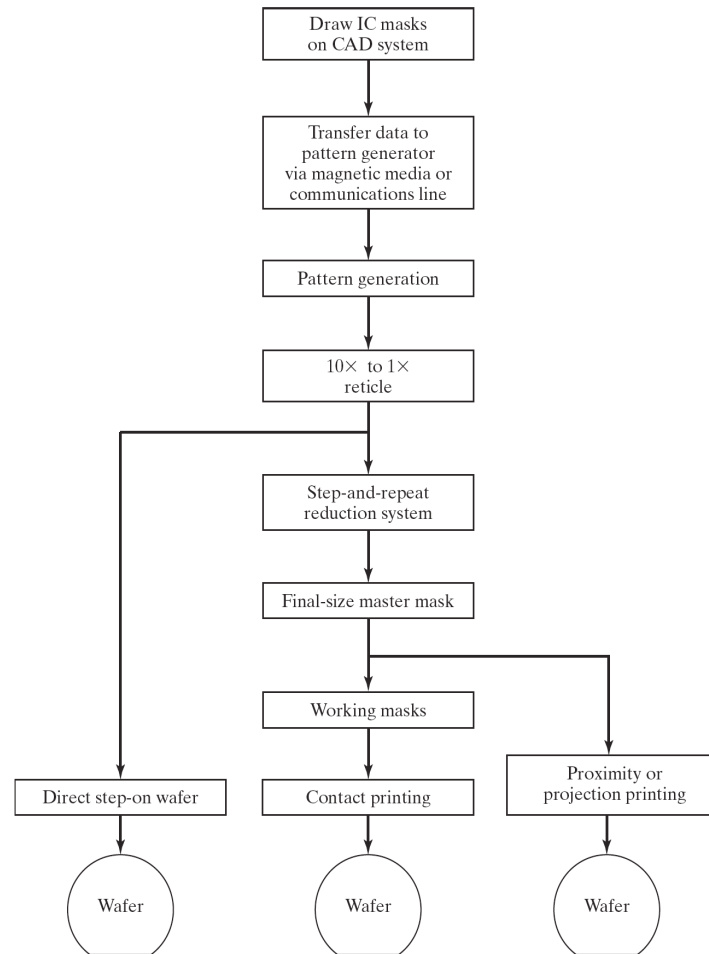


- Contact printing damages the reticle and limits the number of times the reticle can be used
- Proximity printing eliminates damage
- Projection printing can operate in reduction mode with direct step-on-wafer, eliminating the need for the reduction step presented earlier

FIGURE 2.11

Artist's conception of various printing techniques. (a) Contact printing, in which wafer is in intimate contact with mask; (b) proximity printing, in which wafer and mask are in close proximity; (c) projection printing, in which light source is scanned across the mask and focused on the wafer. Copyright, 1983, Bell Telephone Laboratories, Incorporated. Reprinted by permission from Ref. [5].

# Mask Fabrication



- Masking processes
  - Direct step on wafer
  - Contact printing
  - Proximity printing
  - Projection printing

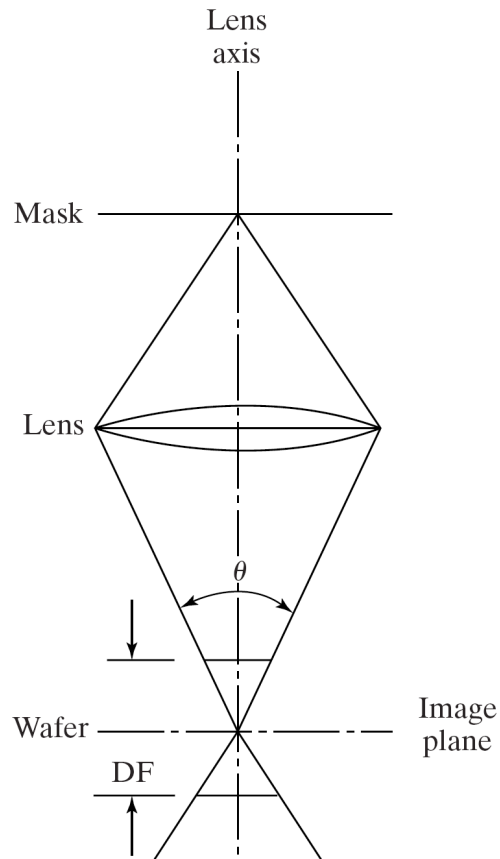
# Wafer Steppers



Figure 2.13 The true complexity of a wafer stepper is apparent in this system drawing. (Courtesy of ASM Lithography, Inc.)

- Wafer stepping systems widely used
- Must be completely isolated from sources of vibration
- High degree of environmental control needed
- Often in their own clean room

# Minimum Feature Size and Depth of Field



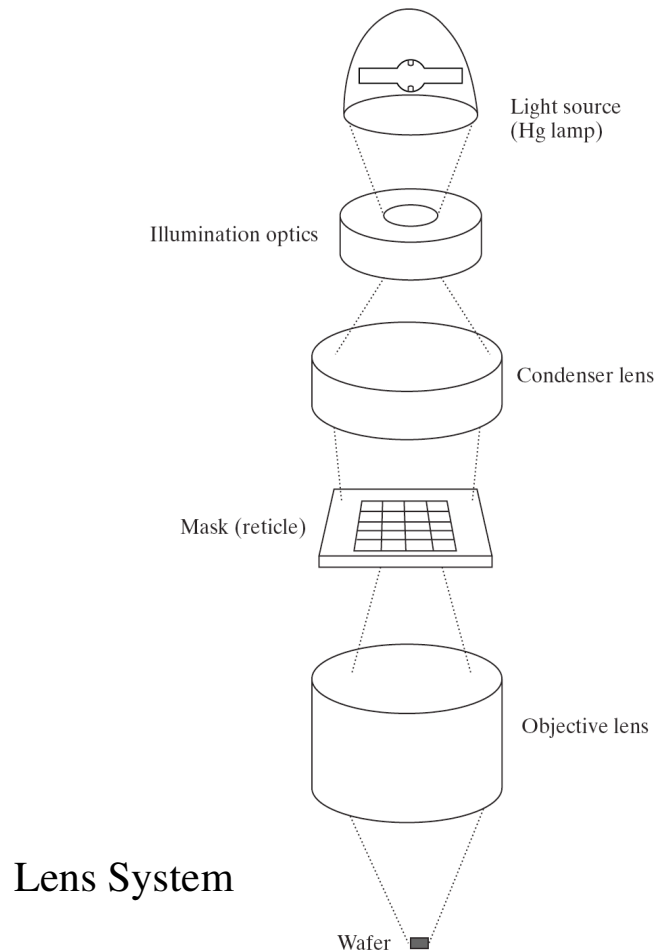
$$\text{Minimum Feature Size } F = 0.5 \frac{\lambda}{NA}$$

$$\text{Depth of Field } DF = 0.6 \frac{\lambda}{(NA)^2}$$

$$\text{Numerical Aperture } NA = \sin \theta$$

$\lambda$  = wavelength of exposure source

# Wafer Steppers (cont.)



Lens System

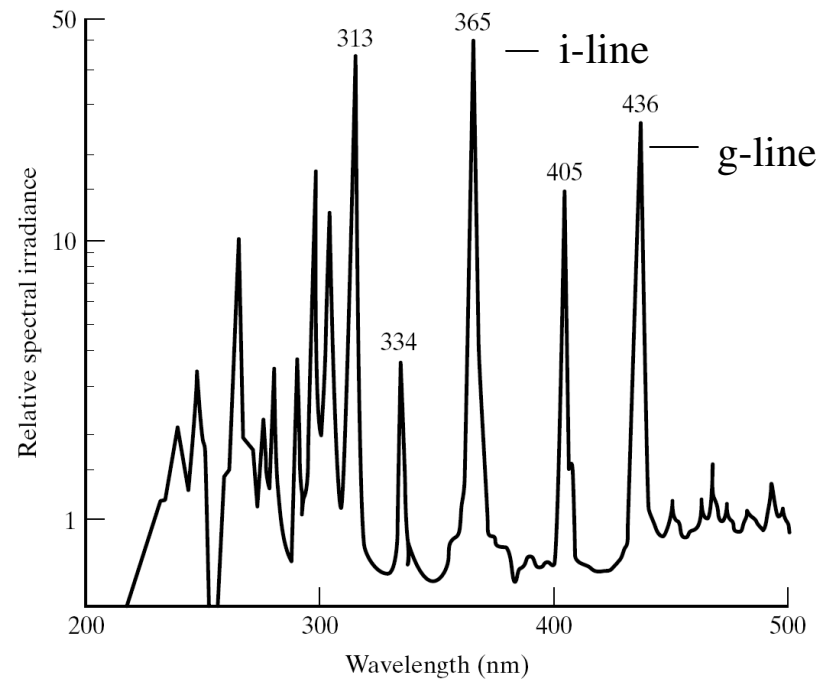
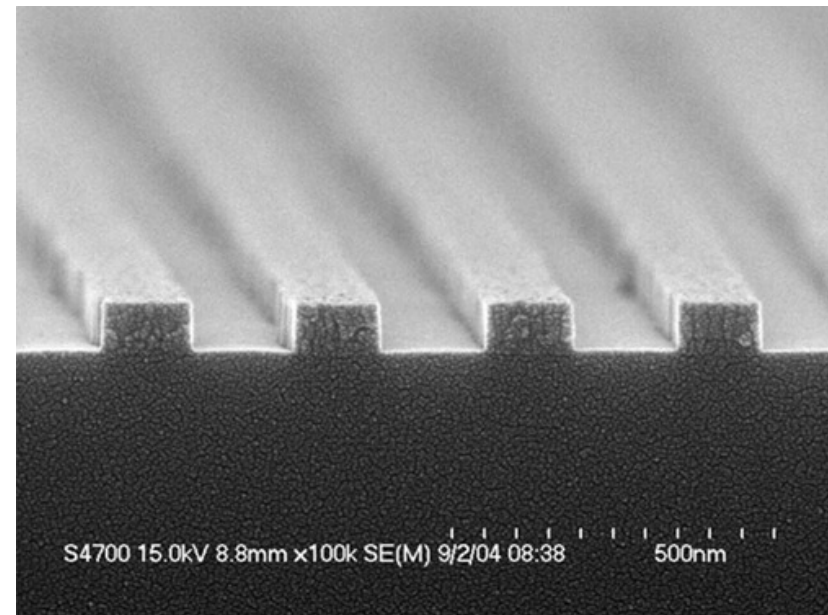


Figure 2.15  
Spectral Content of Xe-Hg lamp (Courtesy of SVG)

# Critical Dimensions

- the width of a patterned line or the distance between two lines, monitored to maintain [device](#) performance consistency; that dimension of a specified geometry that must be within design tolerances.



# Analogy to photography



- Toy camera
- Small lens, small NA



- Large camera
- Large lens, large NA



# Depth of Field



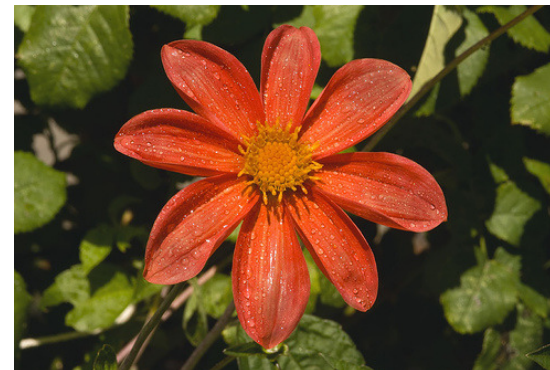
f/4



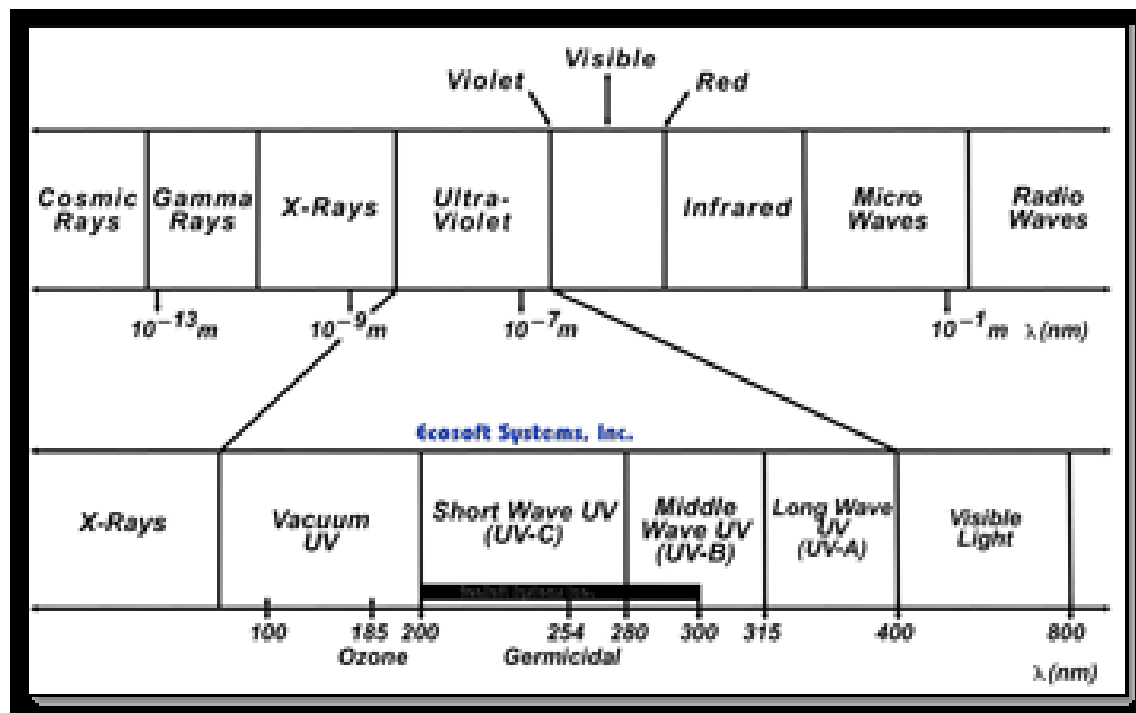
Large DOF

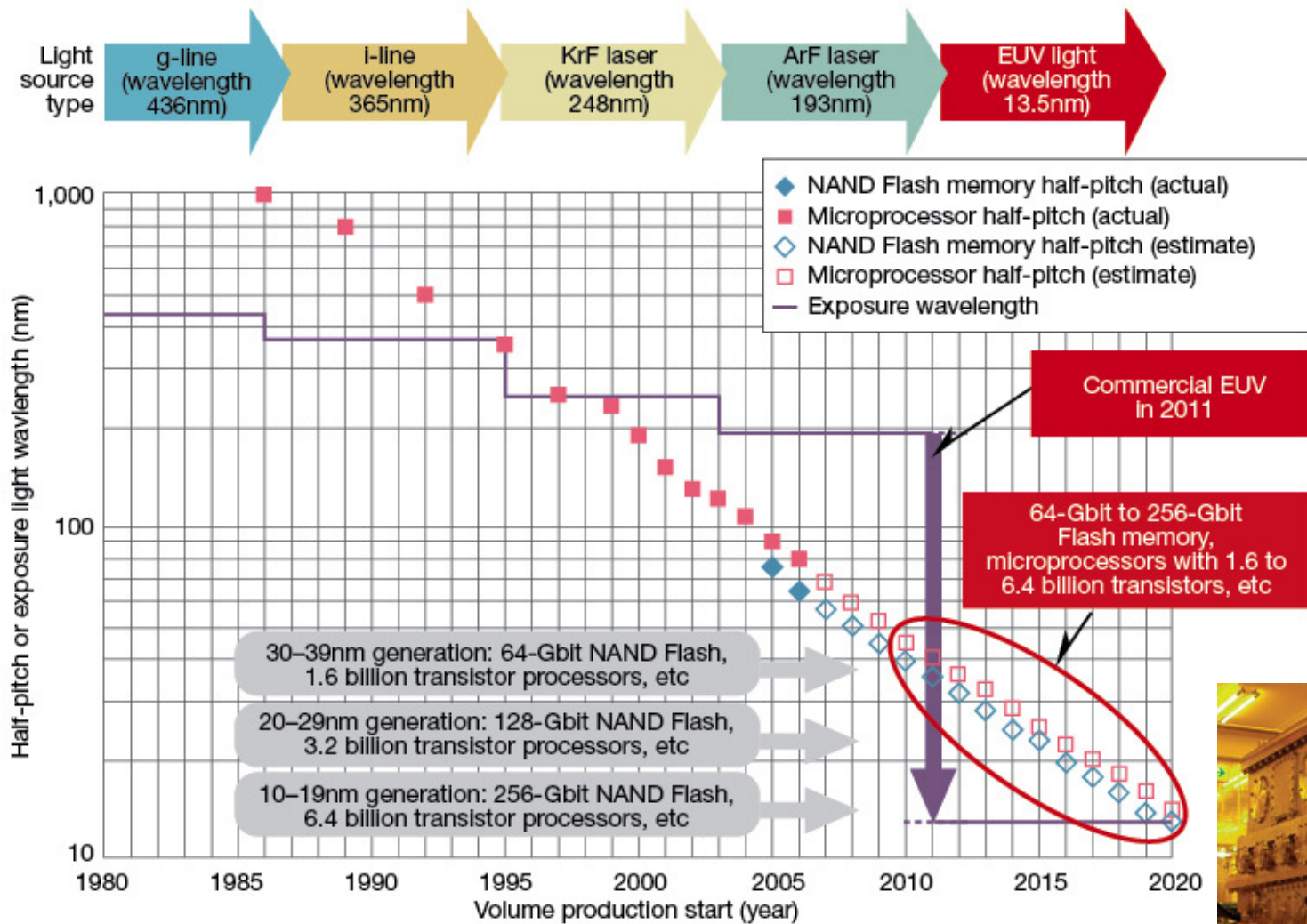


Small DOF



f/32



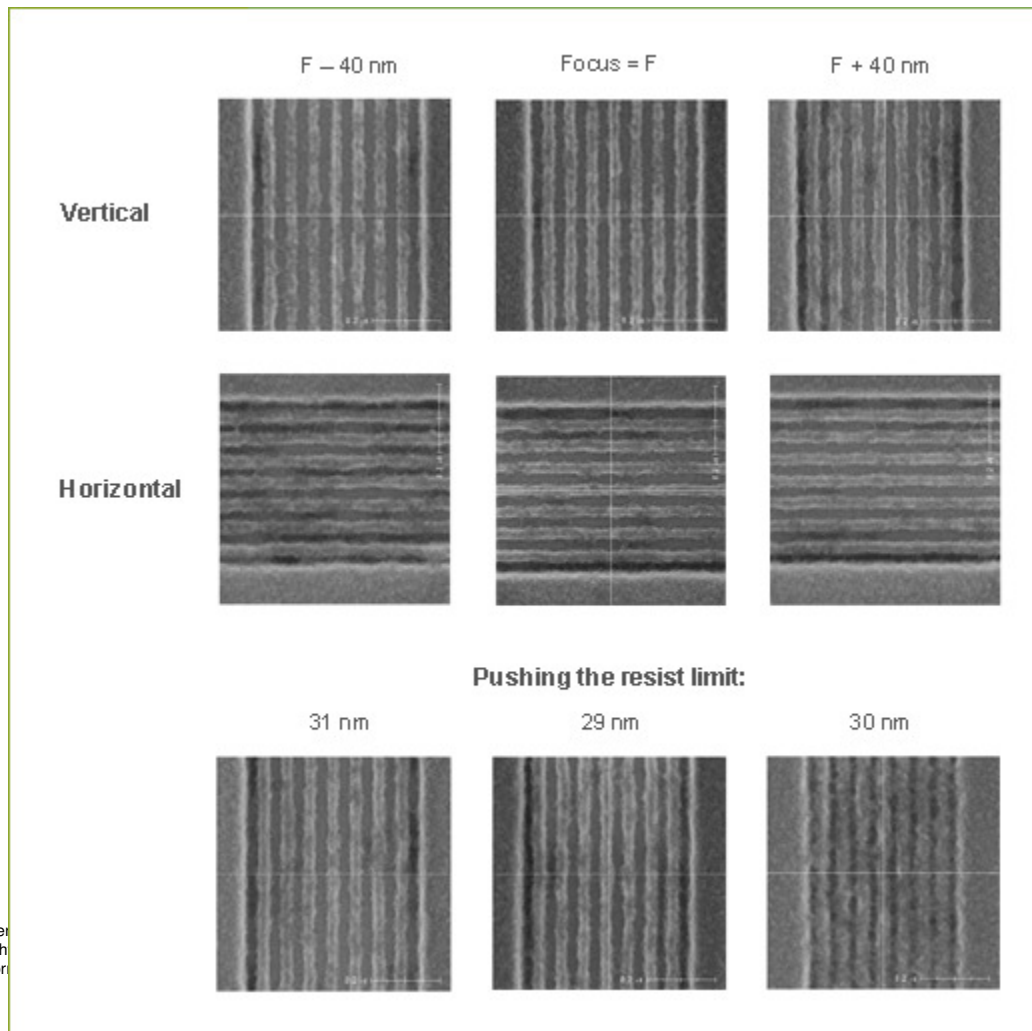


**Fig 1 Slashing Lithography Wavelength to Drive Further Geometry Shrink** EUV lithography has been pegged as a technology for the future, but it is approaching practical use fast. Diagram by *Nikkei Electronics* based on material from Intel, International Technology Roadmap for Semiconductors (ITRS), etc.



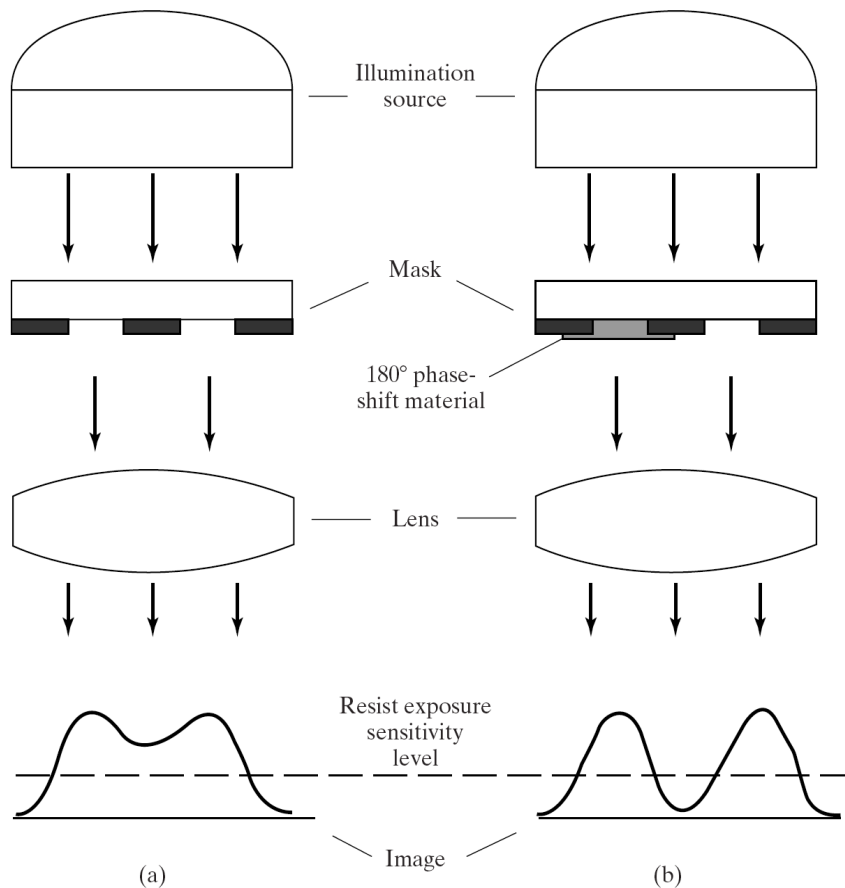
Nikon EUV machine prototype

# EUV Capabilities





# Phase Shifting Masks

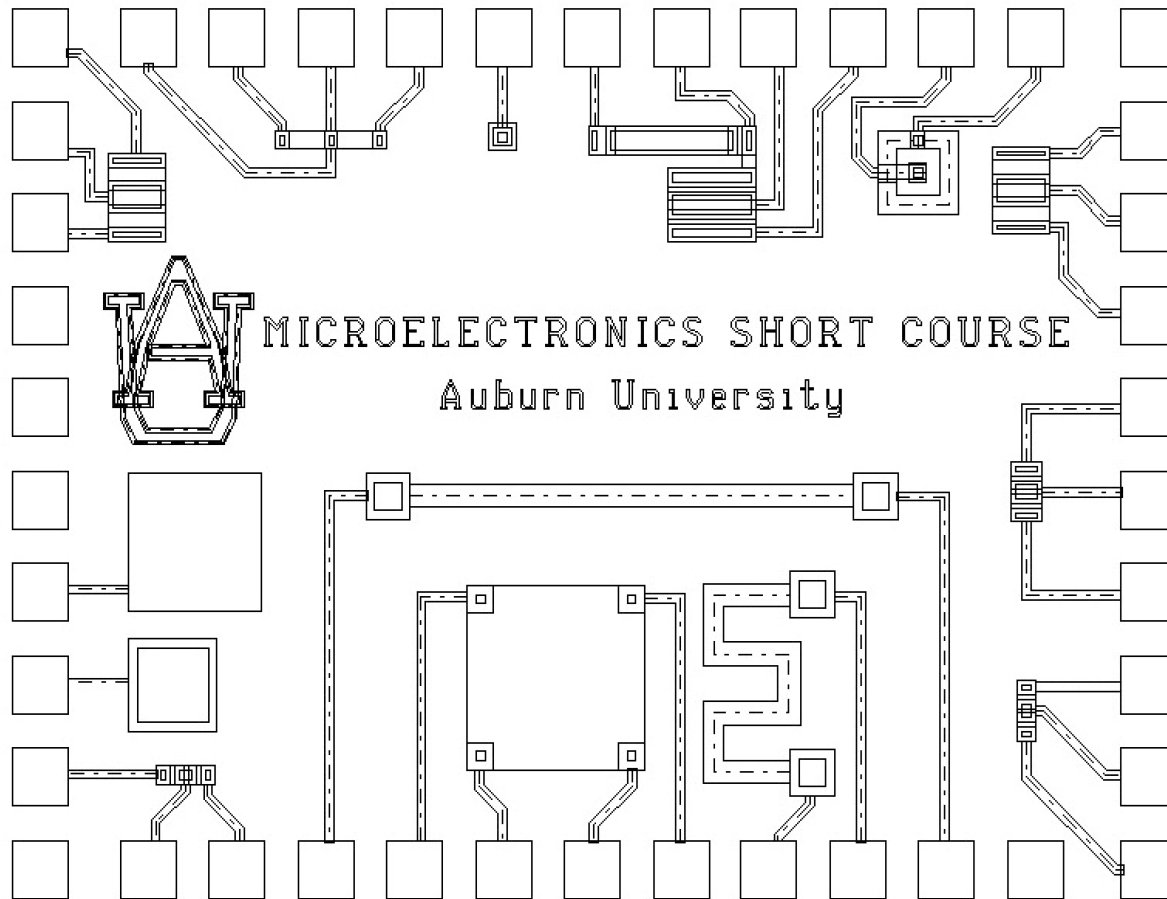


Pattern transfer of two closely spaced lines

(a) Conventional mask technology - lines not resolved

(b) Lines can be resolved with phase-shift technology

# Layout of a Class Chip



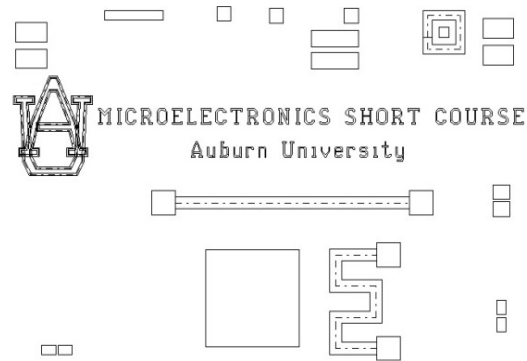
Basic 4-Mask Process

PMOS Metal-Gate Process

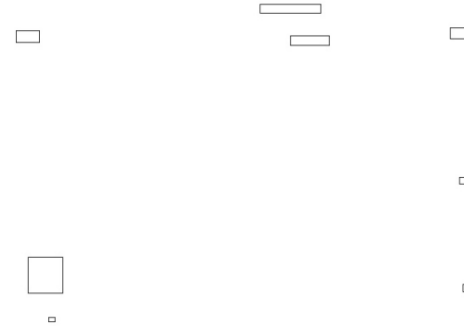
1. p-diffusion
2. Thin oxide
3. Contacts
4. Metal

# Four Mask Class Process

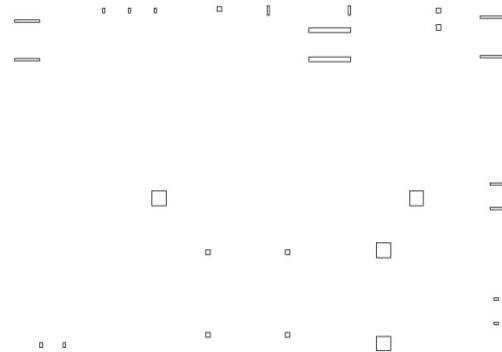
p-diffusion



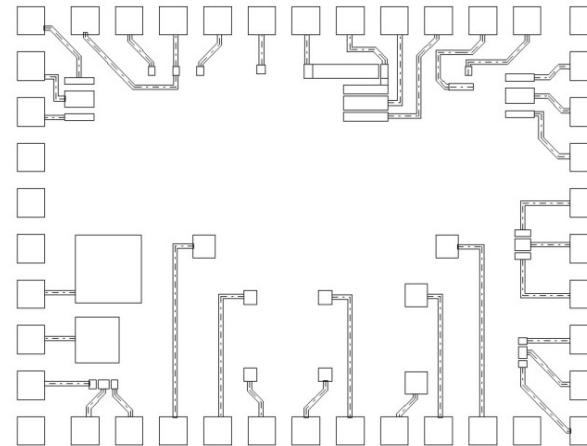
Thin oxide



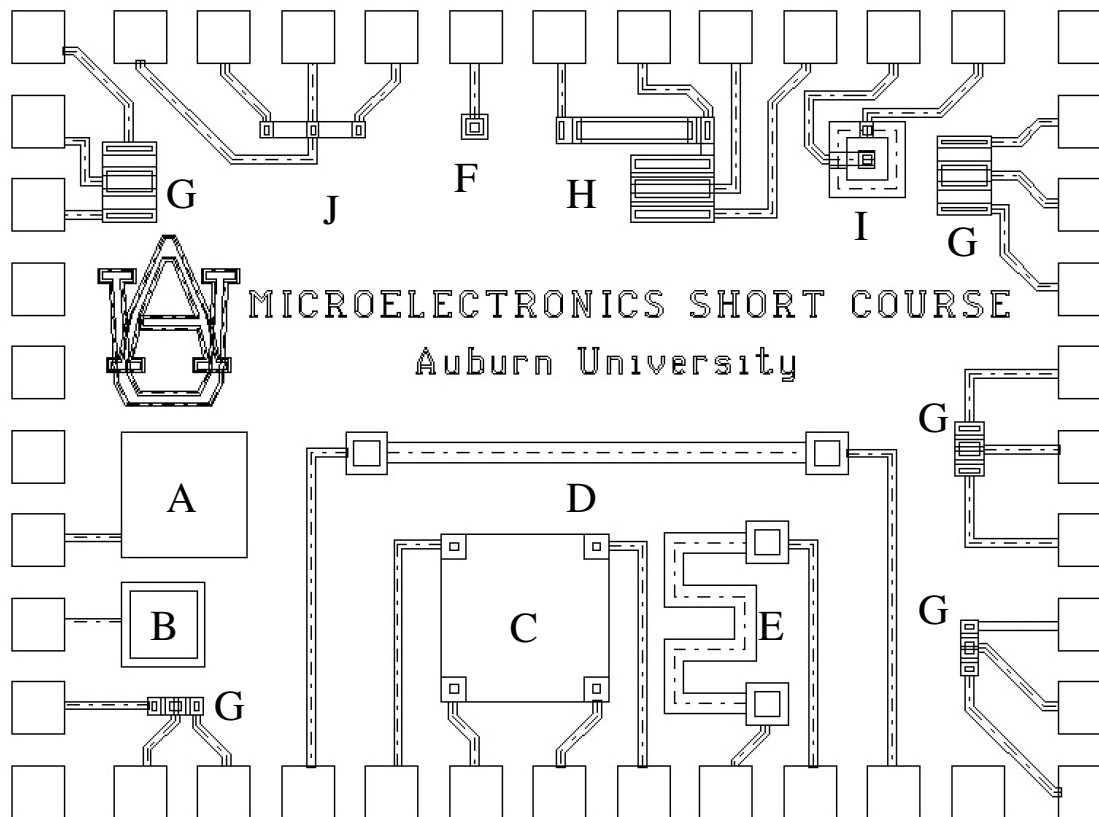
Contacts



Metal



# Layout of Class Chip



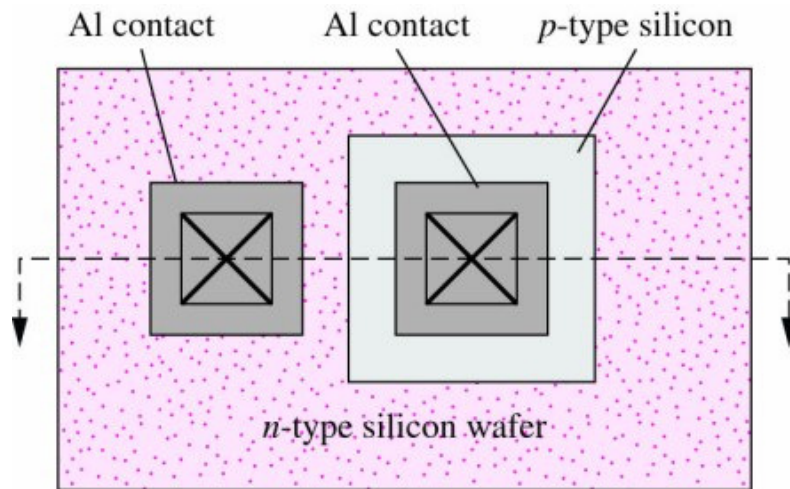
## Metal Gate PMOS Process

- A. Thick oxide capacitor
- B. Thin Oxide Capacitor
- C. Van der Pauw structure
- D. Resistor 1
- E. Resistor 2
- F. Diode
- G. PMOS transistors
- H. PMOS logic inverter
- I. Lateral pnp transistor
- J. Kelvin contact structure



# Our Class Process

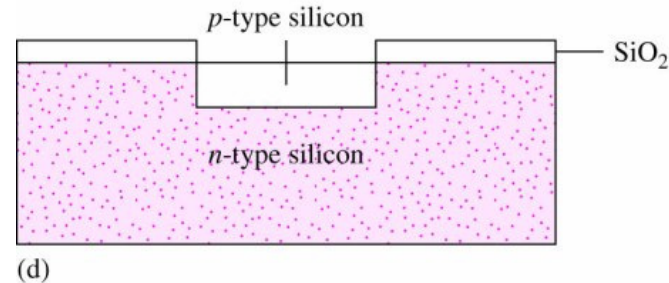
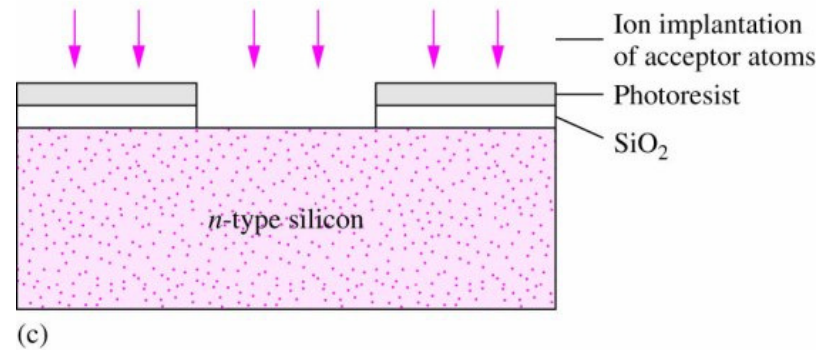
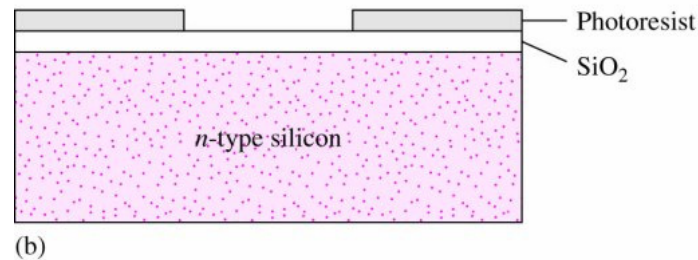
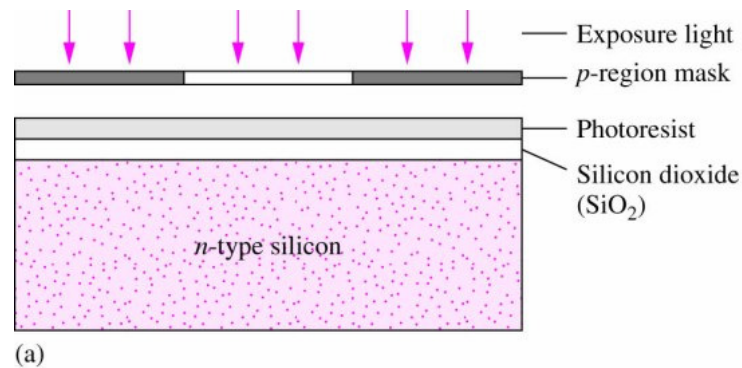
## Diode & Resistor Fabrication



Top view of an integrated pn diode.

# Our Class Process

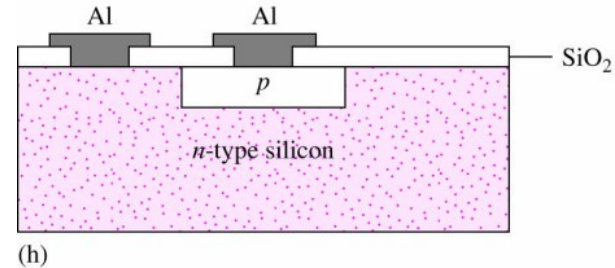
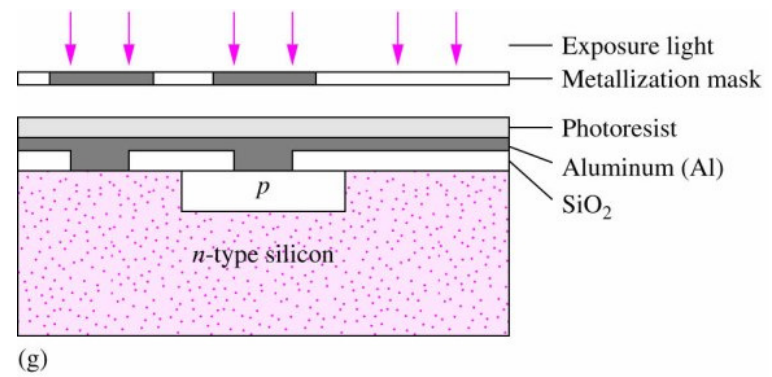
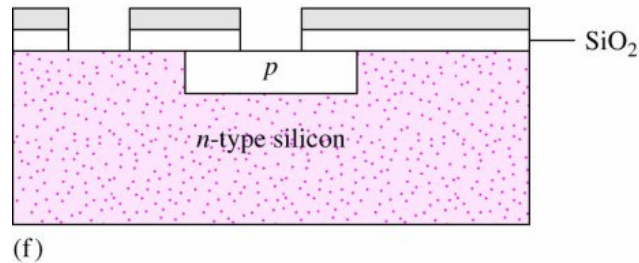
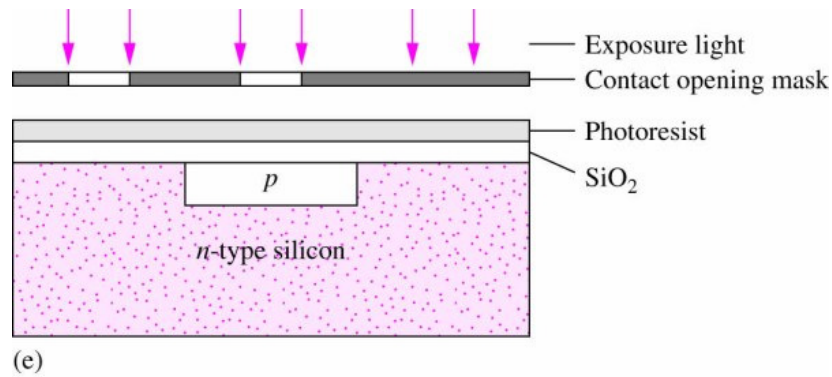
## Diode Fabrication (cont.)



- (a) First mask exposure (b) Post-exposure and development of photoresist  
 (c) After  $\text{SiO}_2$  etch (d) After implantation/diffusion of acceptor dopant.

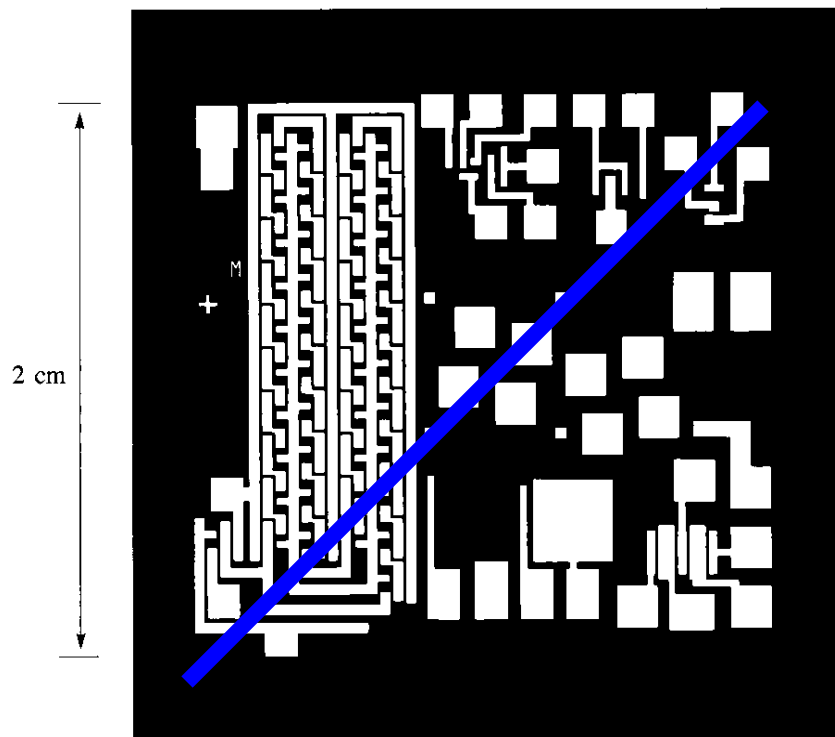
# Our Class Process

## Diode Fabrication (cont.)



(e) Exposure of contact opening mask, (f) after resist development and etching of contact openings, (g) exposure of metal mask, and (h) After etching of aluminum and resist removal.

# Contamination



(b)

- Human hair at the same scale as the integrated circuit with  $10\ \mu\text{m}$  feature size
- Today's feature size  $100\ \text{nm}$  - 100 times smaller!

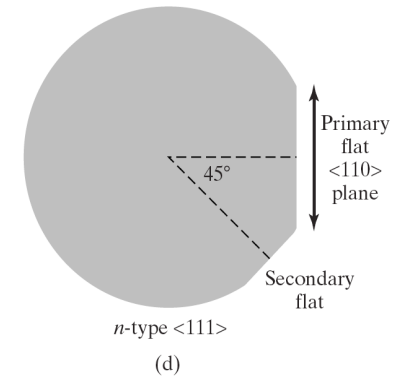
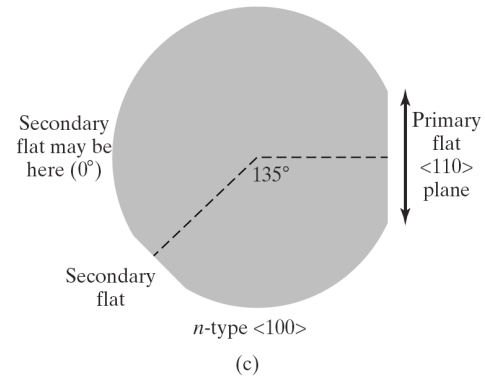
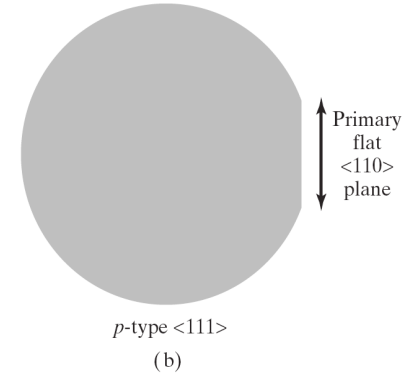
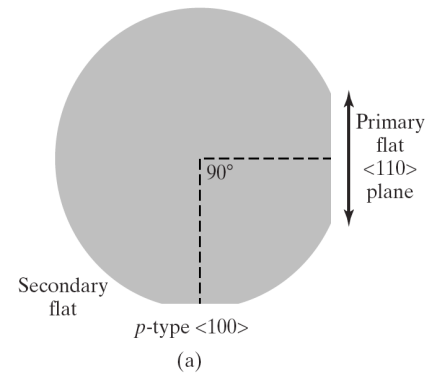
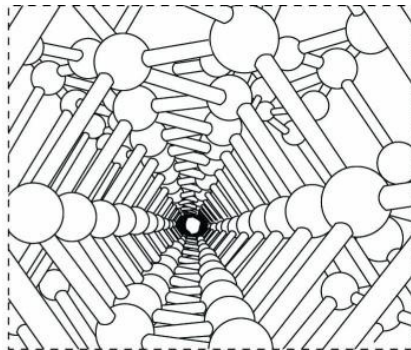
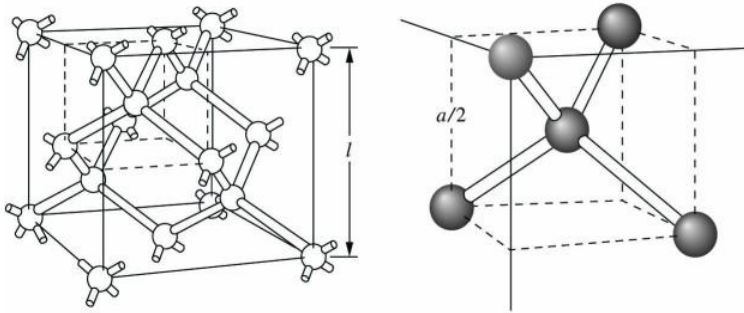
# Clean Room Specifications

Table 2.1      Clean Room Ratings by Class of Filtration

Class	Number of 0.5- $\mu\text{m}$ particles per $\text{ft}^3$ ( $\text{m}^3$ )	Number of 5- $\mu\text{m}$ particles per $\text{ft}^3$ ( $\text{m}^3$ )
10,000	10000 (350,000)	65 (23,000)
1,000	1000 (35,000)	6.5 (2,300)
100	100 (3,500)	0.65 (230)
10	10 (350)	0.065 (23)
1	1 (35)*	0.0065 (2.3)

\*It is very difficult to measure particulate counts below  $10/\text{ft}^3$

# Common Wafer Surface Orientations



# End of Chapter 2