Introduction to Microelectronic Fabrication

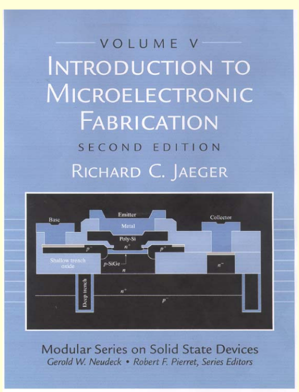
by

Richard C. Jaeger

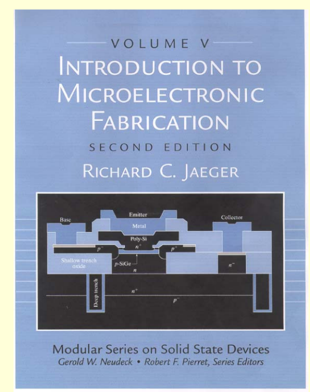
Distinguished University Professor

ECE Department

Auburn University



Chapter 1
An Overview of Microelectronic Fabrication



For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

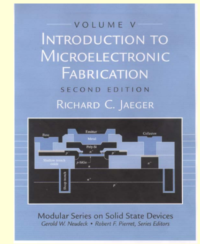
Copyright Notice

- For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

© 2002 Pearson Education, Inc., Upper Saddle River, NJ. All rights reserved. This material is protected under all copyright laws as they currently exist. No portion of this material may be reproduced, in any form or by any means, without permission in writing from the publisher.

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Historical Trends
Silicon Wafer Size



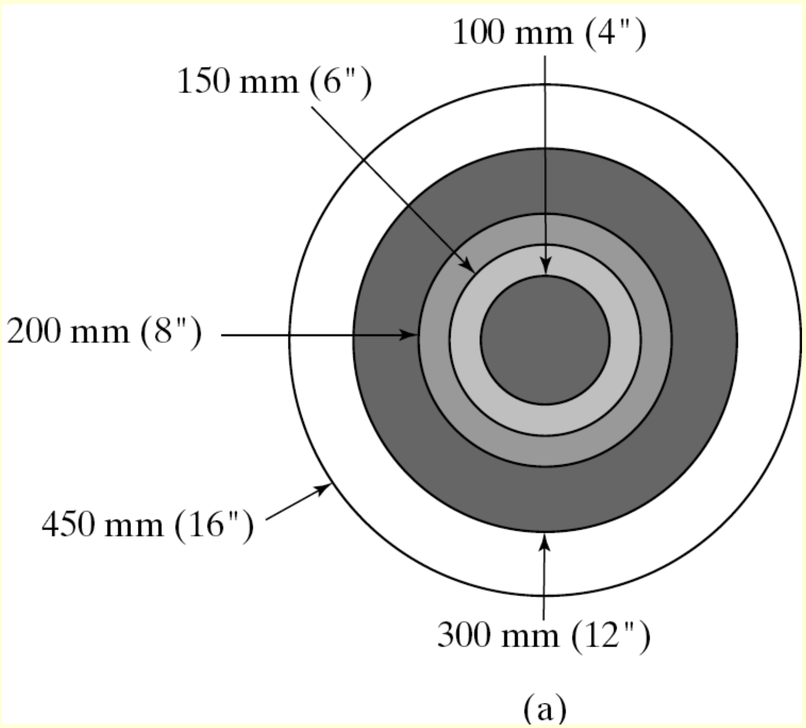


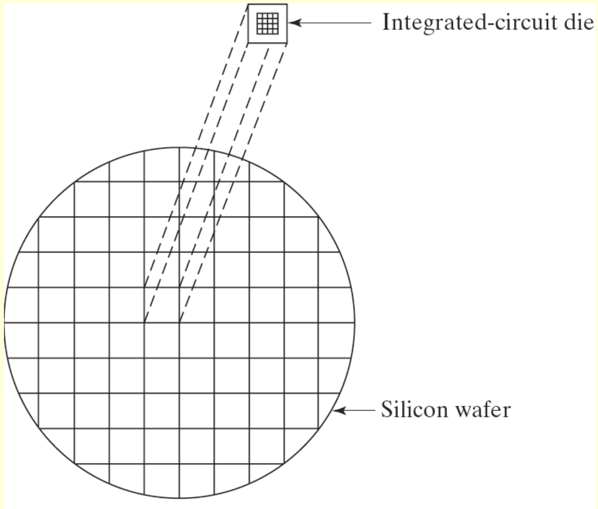
FIGURE 1.1

(a) Relative size of wafers with diameters ranging from 100 to 450 mm; (b) The same integrated circuit die is replicated hundreds of times on a typical silicon wafer; (c) the graph gives the approximate number of 10 x 10 mm dice that can be fabricated on wafers of different diameters.

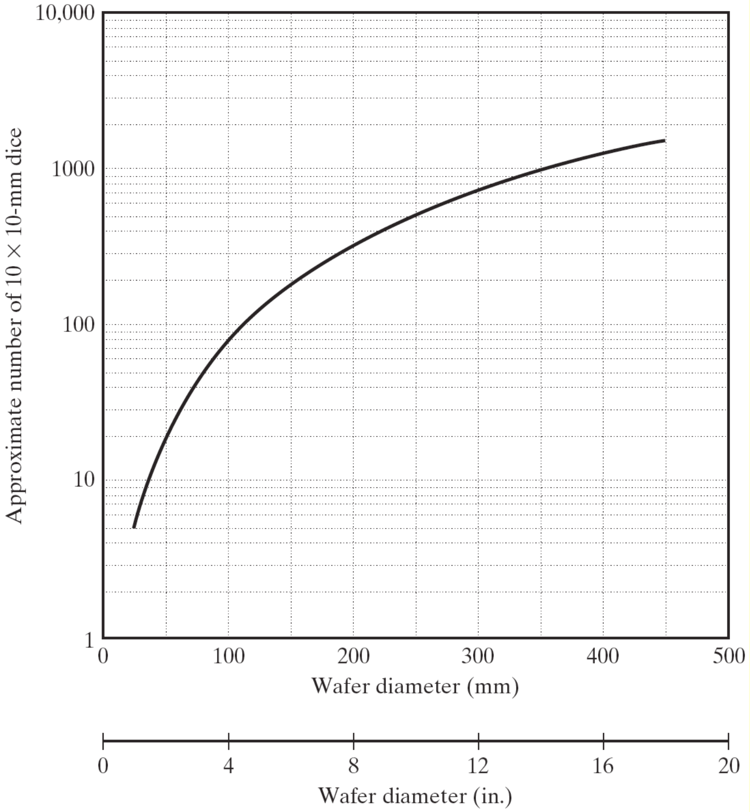
- Early Wafers - 1, 1.5, 2 Inch Diameters
- Wafer Size has Increased Steadily
- 200 mm (8”) Wafers in Production
- 300 mm (12”) Coming on Line Now (> 3B$/Fab)
- 450 mm Planned

Larger Wafers

Lower Die Cost



(b)

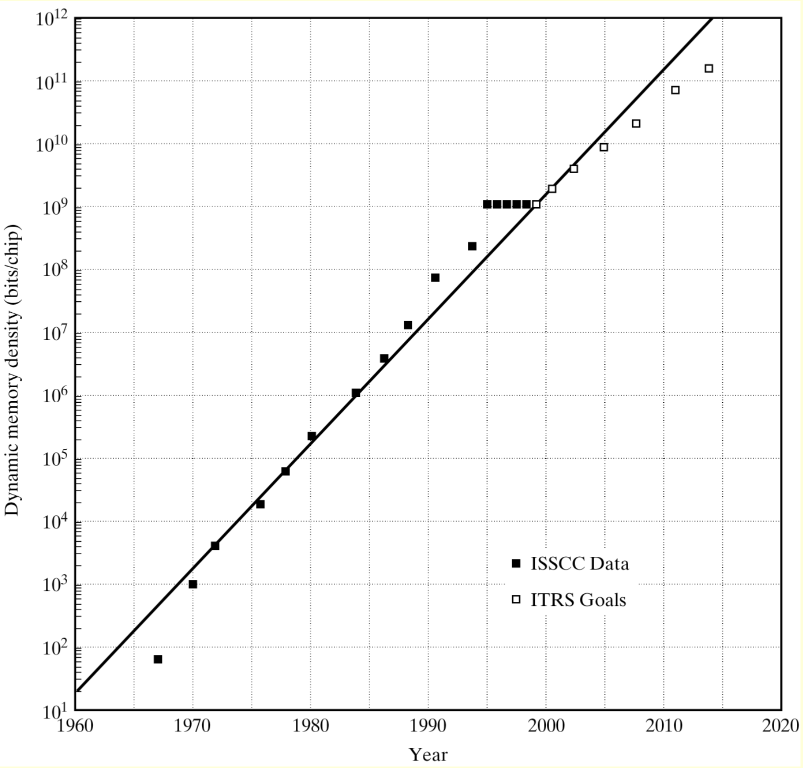


(c)

- Cost to Process a Wafer is Relatively Fixed for a Given Process
- Larger Wafer →Lower Cost/Die

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Historical Trends
Memory Density (Bits/Chip)



- Moore's Law - Exponential Increase in Chip Complexity
- ISSCC Research Benchmarks
  - 1967 - 64 bit Memory
  - 1984 - 1Mb Memory
  - 1995 - First 1 Gb Memory

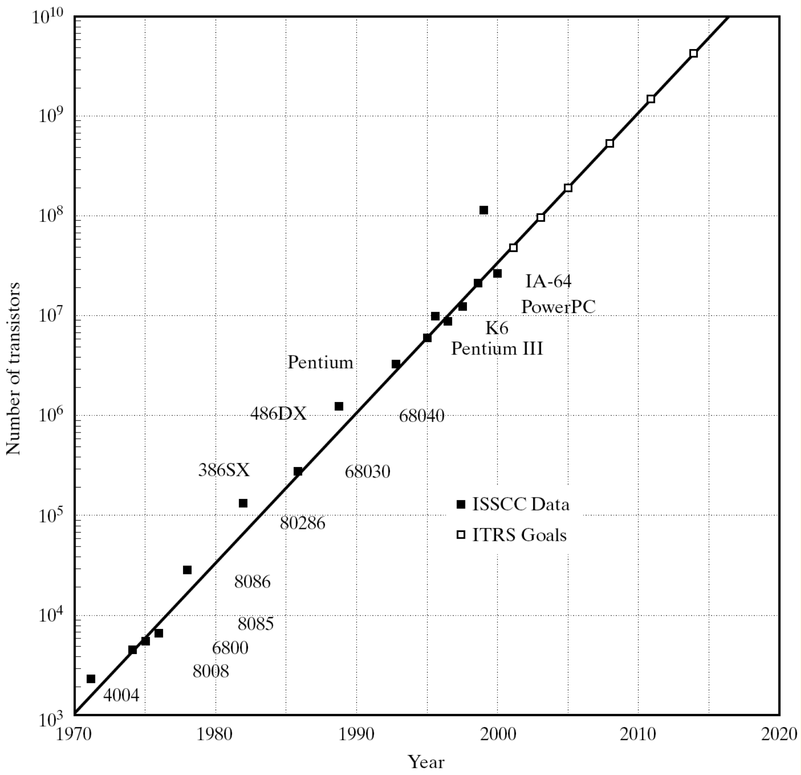
FIGURE 1.2

(a) Dynamic memory density versus year since 1960.

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Historical Trends

Microprocessor Complexity (Trans./Chip)



- ISSCC Benchmarks
  - 1971 - 2000 Transistors
  - 1988 - 1M Transistors
  - 1998 - 100M Transistors

FIGURE 1.2

(b) Number of transistors in a microprocessor versus year.

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Semiconductor Industry Roadmap - ITRS

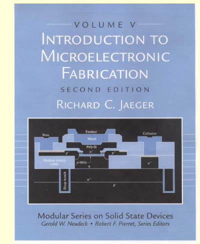
TABLE 1.1 International Technology Road Map for Semiconductors (ITRS) [4]

	Selected Projections					
Year of First Product Shipment	2001	2003	2005	2008	2011	2014
DRAM Metal Line Half-Pitch (nm)	150	120	100	70	50	35
Microprocessor Gate Widths (nm)	100	80	65	45	30	20
DRAM (G-bits/chip)	2.2	4.3	8.6	24	68	190
Microprocessor (M-transistors/chip)	48	95	190	540	1500	4300
DRAM Chip Area: Year of Introduction (mm^2)	400	480	526	600	690	790
DRAM Chip Area: Production (mm^2)	130	160	170	200	230	260
MPU Chip Size at Introduction (mm^2)	340	370	400	470	540	620
MPU Chip Area: Second "shrink" (mm^2)	180	210	230	270	310	350
Wafer Size (mm)	300	300	300	450	450	450

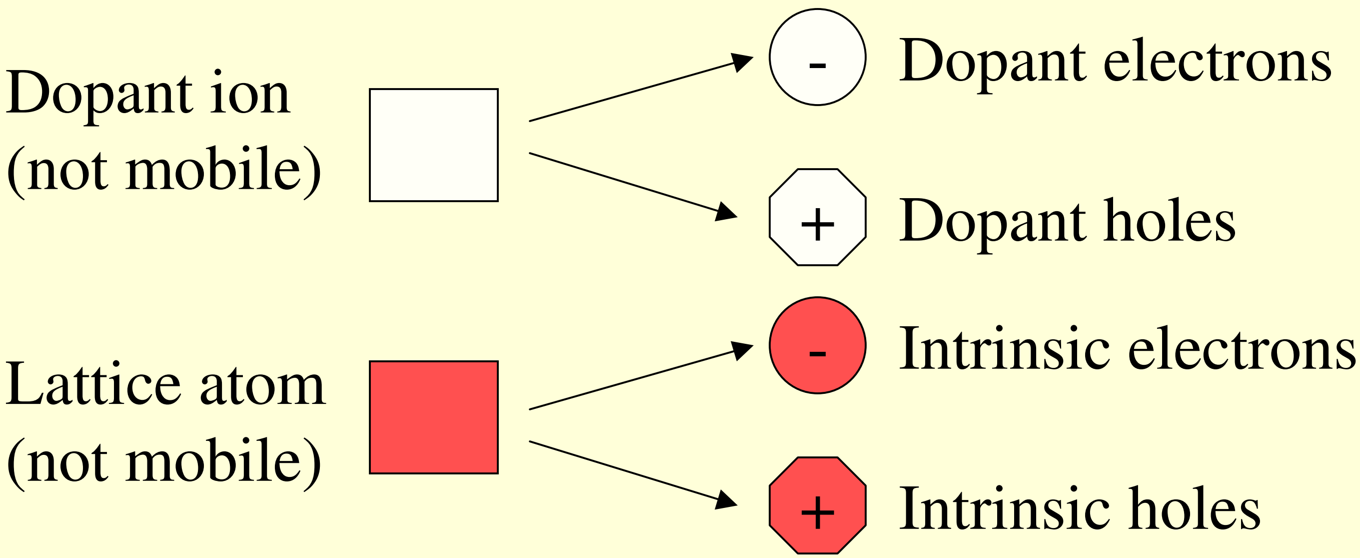
[4] *The International Technology Roadmap for Semiconductors*, The Semiconductor Industry Association (SIA), San Jose, CA, 1999. (http://www.semichips.org)

Each new process generation doubles chip density by scaling feature size by 0.7.

Semiconductor

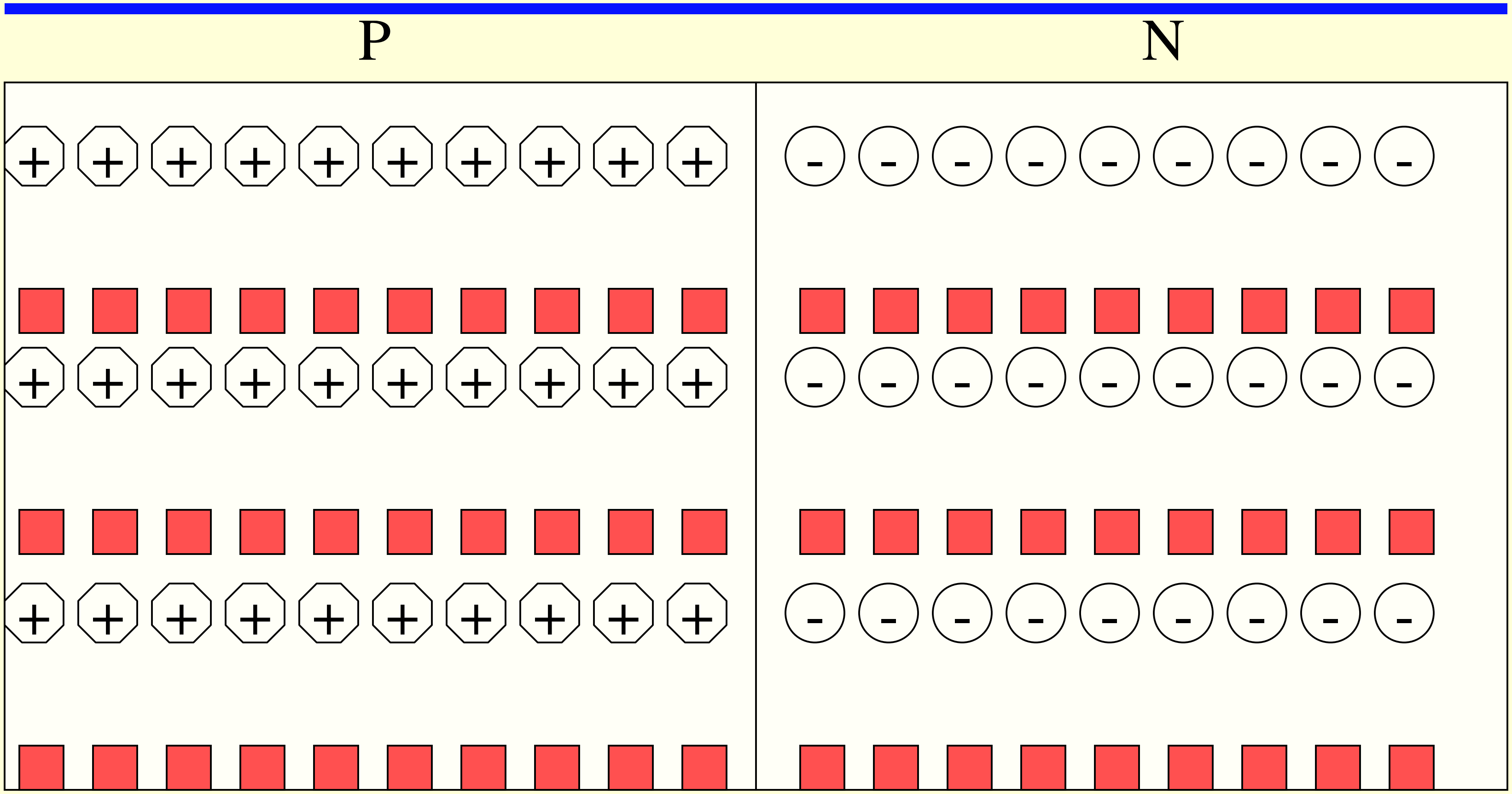


- Six types of charges



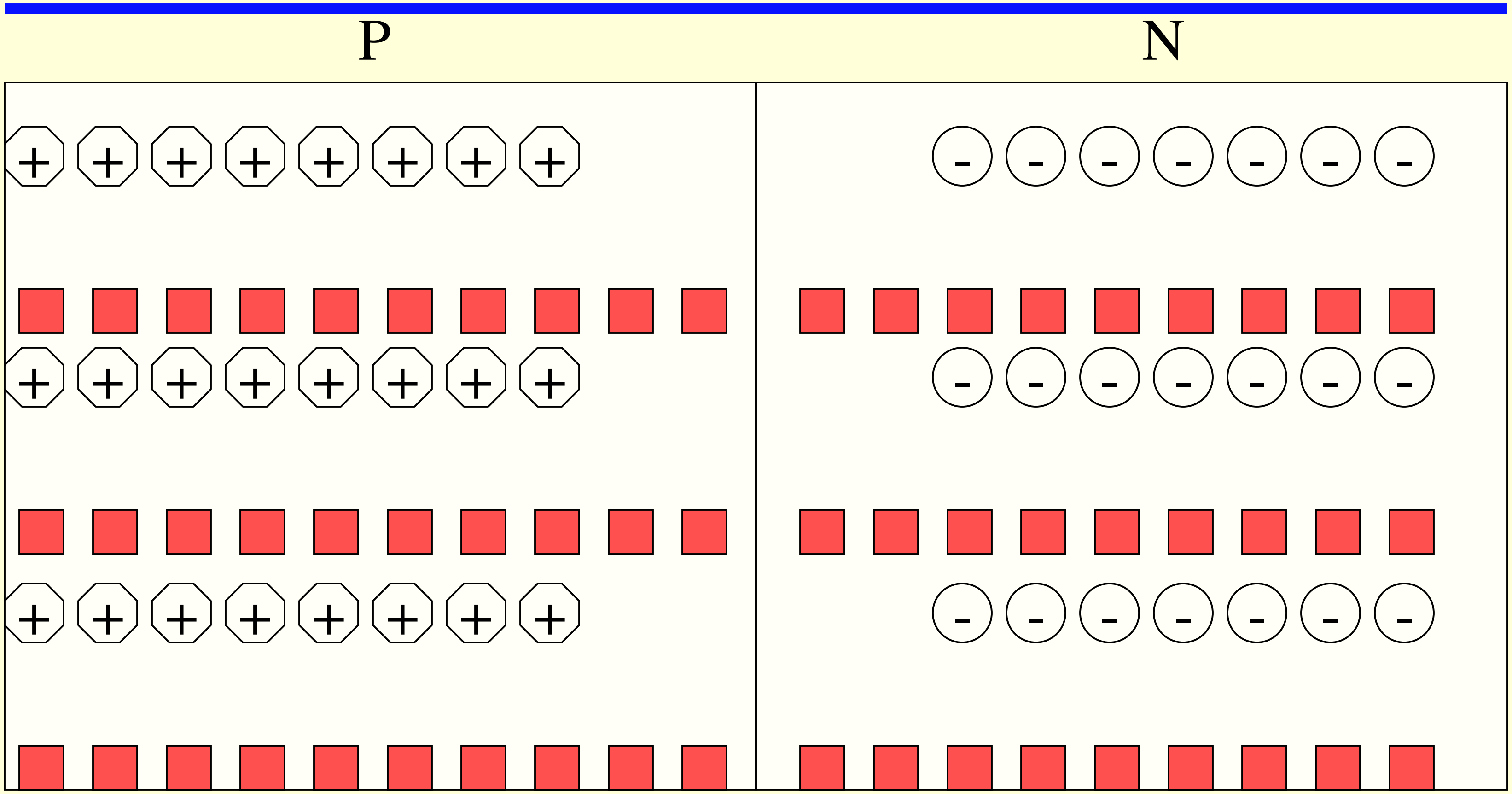
For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Diode – at t=0-



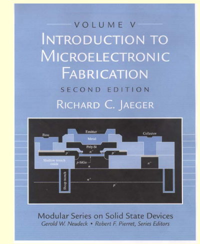
For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

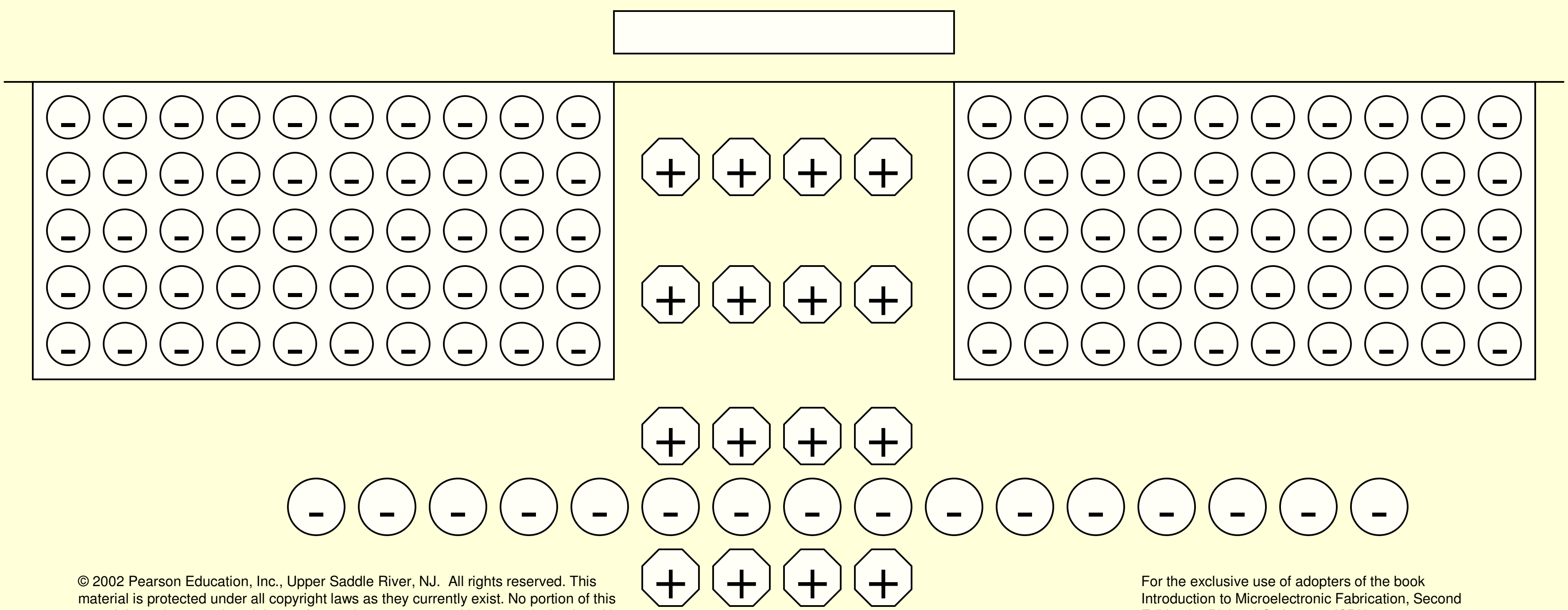
Diode – at t=0+



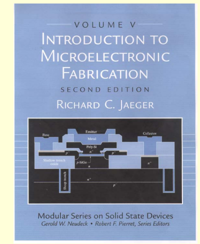
For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

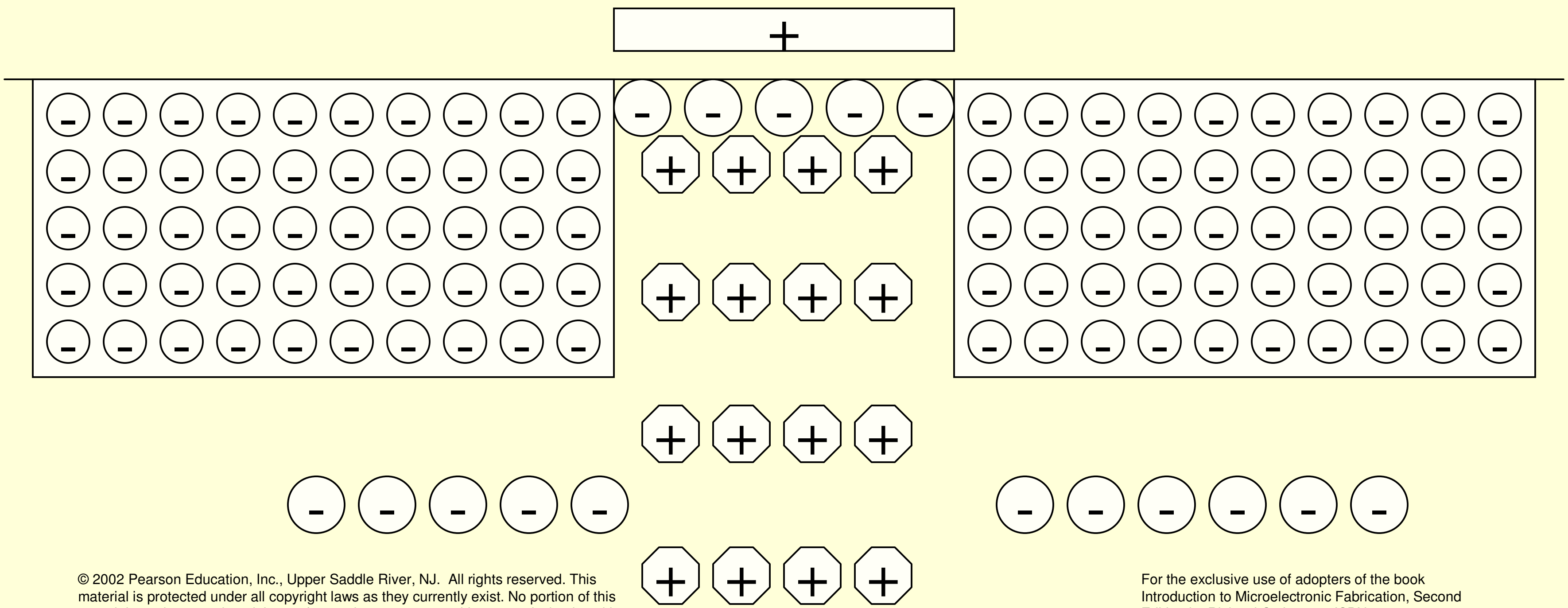
N-MOS Transistor





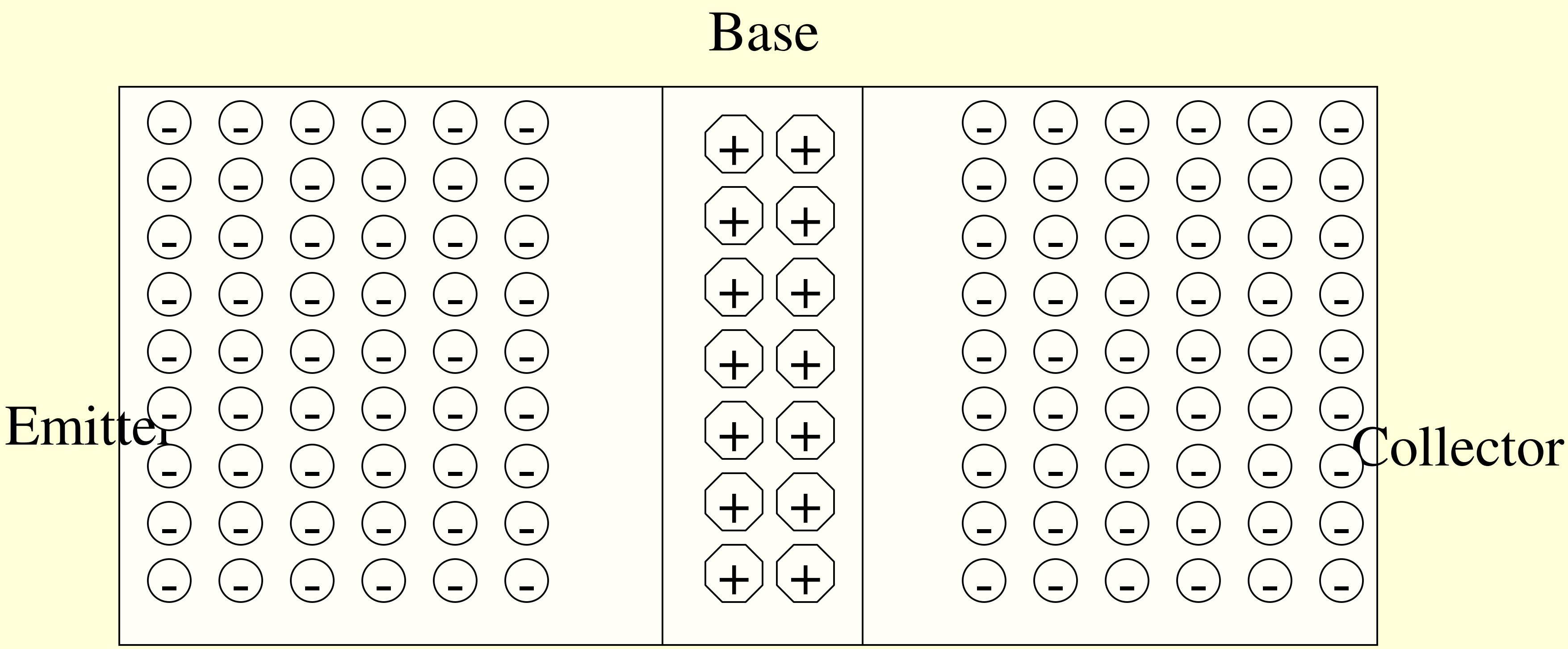
N-MOS Transistor Channel Open





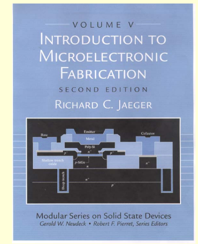
For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

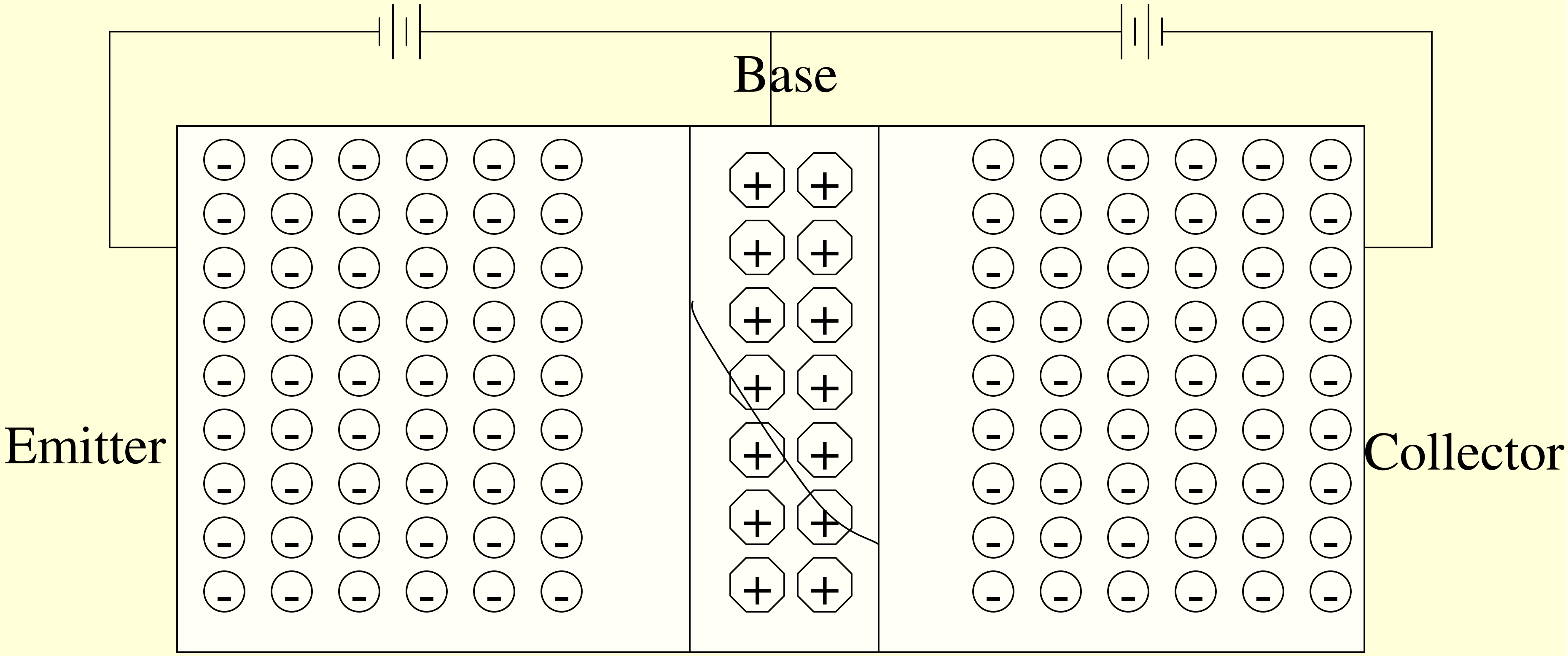
Junction Transistor - NPN, equilibrium



For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

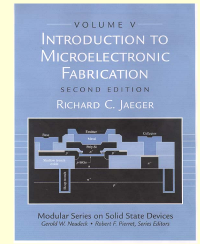
Junction Transistor - NPN, equilibrium





For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

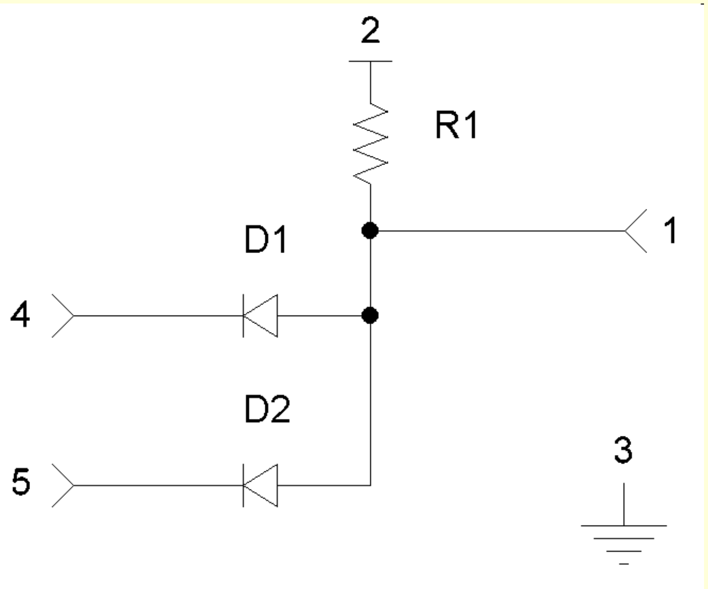
MOS vs. BJT



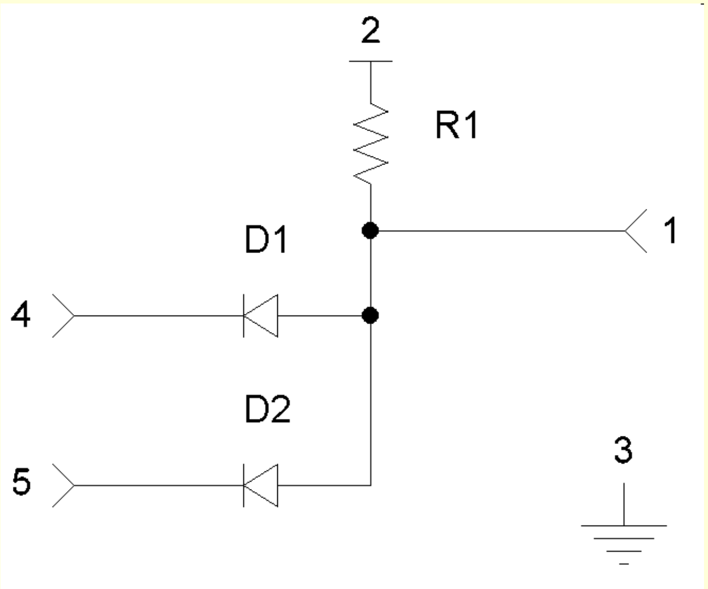
- BJT
  - High speed, high gain, low output resistance
  - Ideal for high frequency amplifier
- CMOS
  - High input impedance
  - Low power logic gate

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Diode Logic



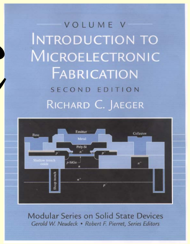
OR Gate

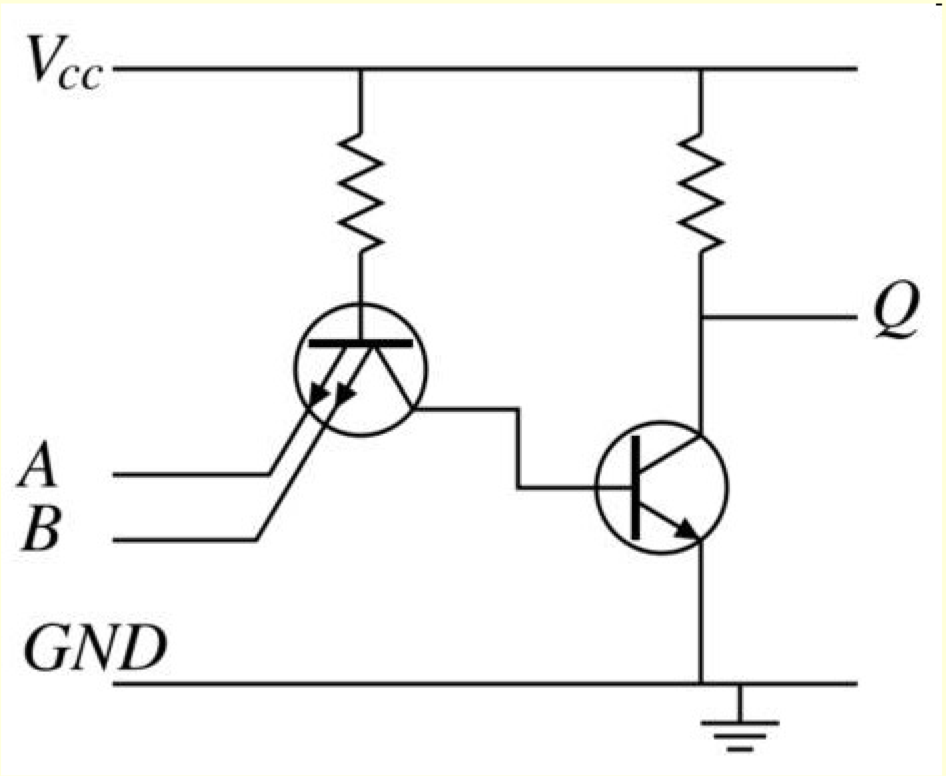


AND Gate

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Transistor-Transistor Logic (TTL)





NAND Gate

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Digital Circuit Elements
Boolean Algebra

∧	0	1
0	0	0
1	0	1

∨	0	1
0	0	1
1	1	1

→	0	1
0	1	1
1	0	1

⊕	0	1
0	0	1
1	1	0

Figure 1. Truth tables

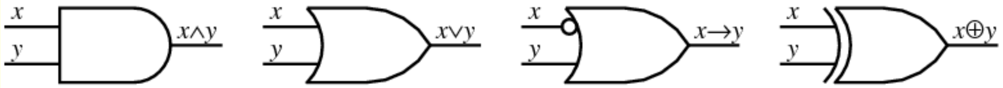


Figure 2. Logic gates

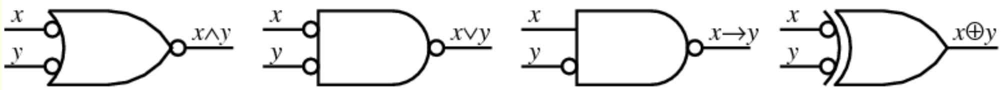
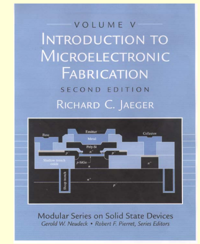


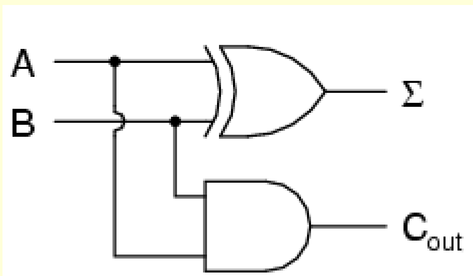
Figure 3. De Morgan equivalents

Figure 4. Venn diagrams

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

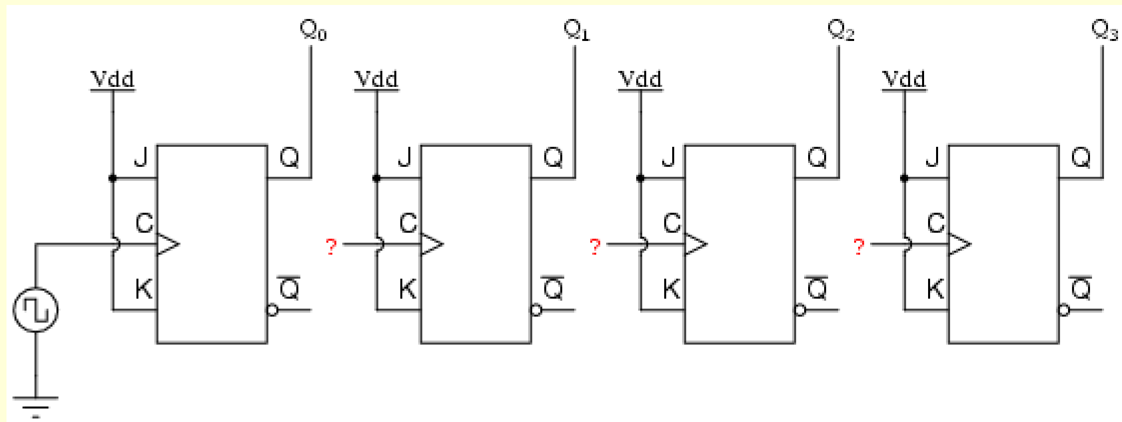
Digital Computing

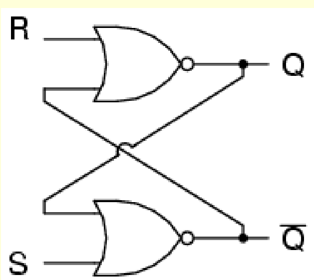




Adder

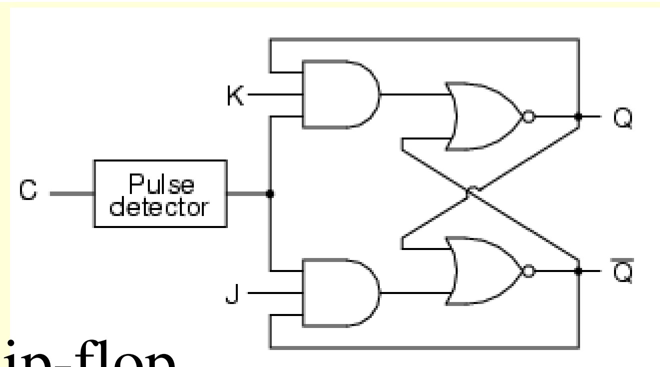
Counter





S	R	Q	$\overline{Q}$
0	0	latch	latch
0	1	0	1
1	0	1	0
1	1	0	0

Latch



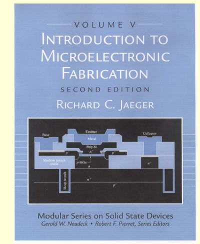
C	J	K	Q	$\overline{Q}$
↑	0	0	latch	latch
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	toggle	toggle
x	0	0	latch	latch
x	0	1	latch	latch
x	1	0	latch	latch
x	1	1	latch	latch

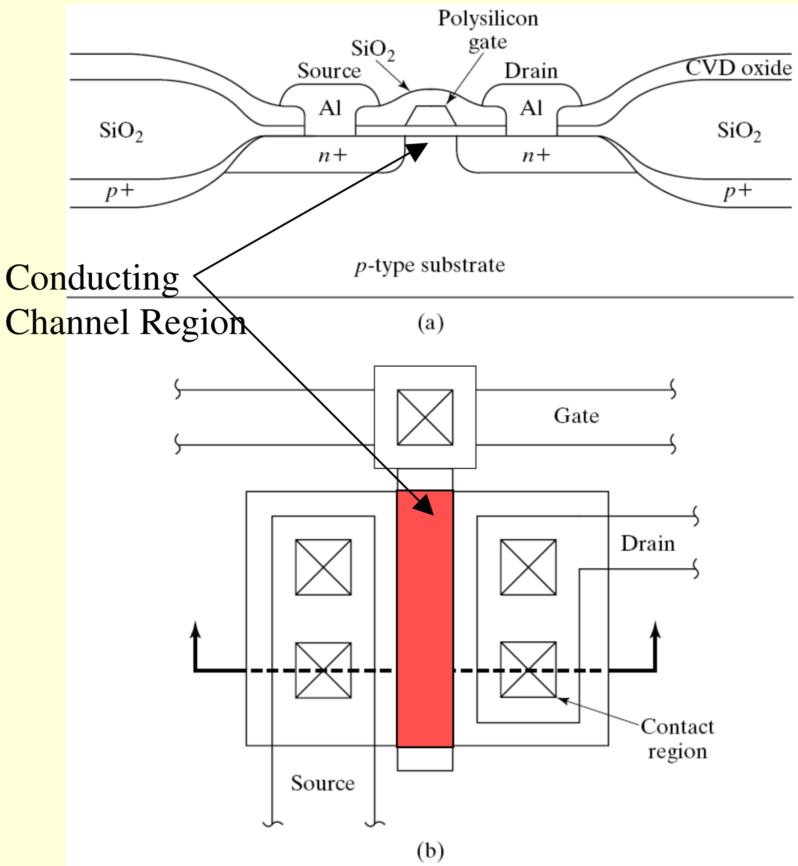
Flip-flop

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

NMOS Transistor

Top View and Cross-Section





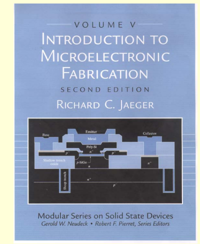
- N-Channel Metal-Oxide Semiconductor Transistor
- n- and p-type semiconductor regions
- Thick and thin oxides
- Etching Openings
- Polysilicon gate
- Metal (Al) Interconnections

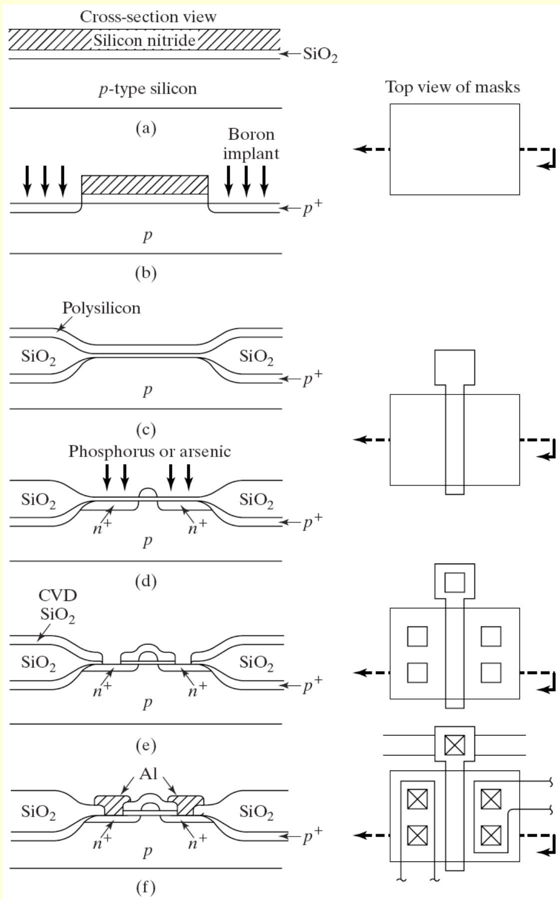
FIGURE 1.4

The basic structure of an n-channel metal-oxide-semiconductor (NMOS) transistor structure. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a). The transistor uses heavily doped polysilicon as the gate "metal."

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Basic NMOS Process
Key Steps

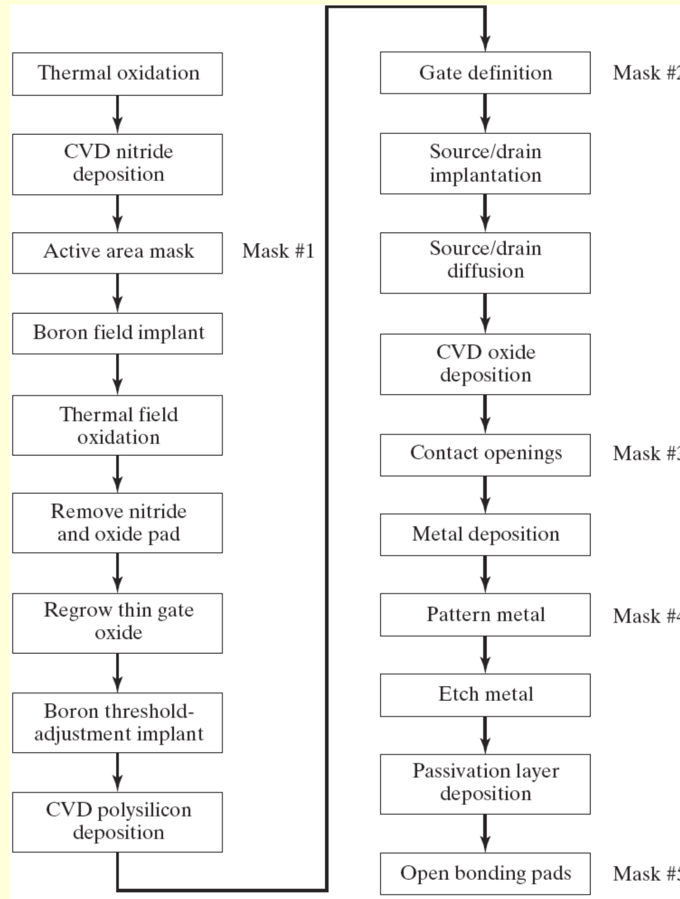




- Oxidation
- Photolithography
- Implantation
- Diffusion
- Etching
- Film Deposition

FIGURE 1.6

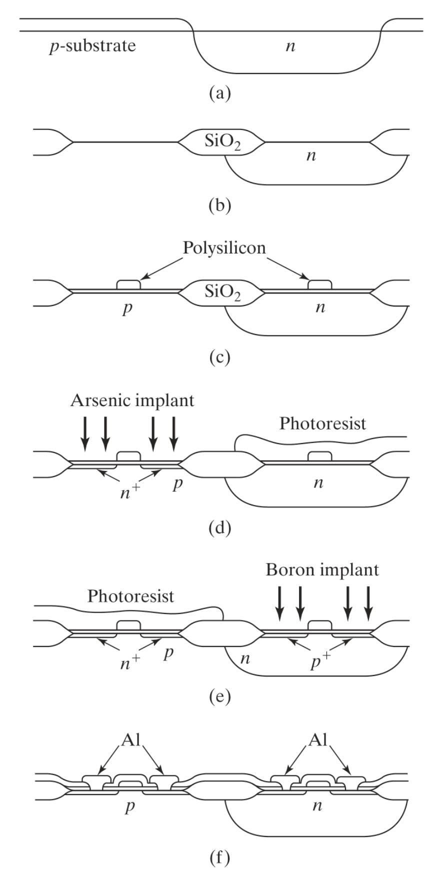
Process sequence for a semirecessed oxide NMOS process. (a) Silicon wafer covered with silicon nitride over a thin padding layer of silicon dioxide; (b) etched wafer after first mask step. A boron implant is used to help control field oxide threshold; (c) structure following oxidation, nitride removal, and polysilicon deposition; (d) wafer after second mask step and etching of polysilicon; (e) the third mask has been used to open contact windows following silicon dioxide deposition; (f) final structure following metal deposition and patterning with fourth mask.



For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

CMOS Technology

N-Well Technology Cross-Section



Oxidation

Photolithography

Implantation

Diffusion

Etching

Film Deposition

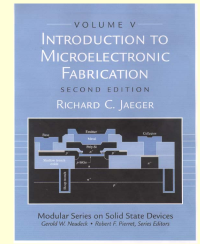
- **C**omplementary **M**etal-**O**xide **S**emiconductor Technology
- Dominant Technology in Integrated Circuits Today!
- Requires both NMOS and PMOS Transistors

FIGURE 1.8

Cross-sectional views at major steps in a basic CMOS process. (a) Following *n*-well diffusion, (b) following selective oxidation, and (c) following gate oxidation and polysilicon gate definition; (d) NMOS source/drain implantation; (e) PMOS source/drain implantation; (f) structure following contact and metal mask steps.

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Bipolar Transistor
Top View and Cross-Section



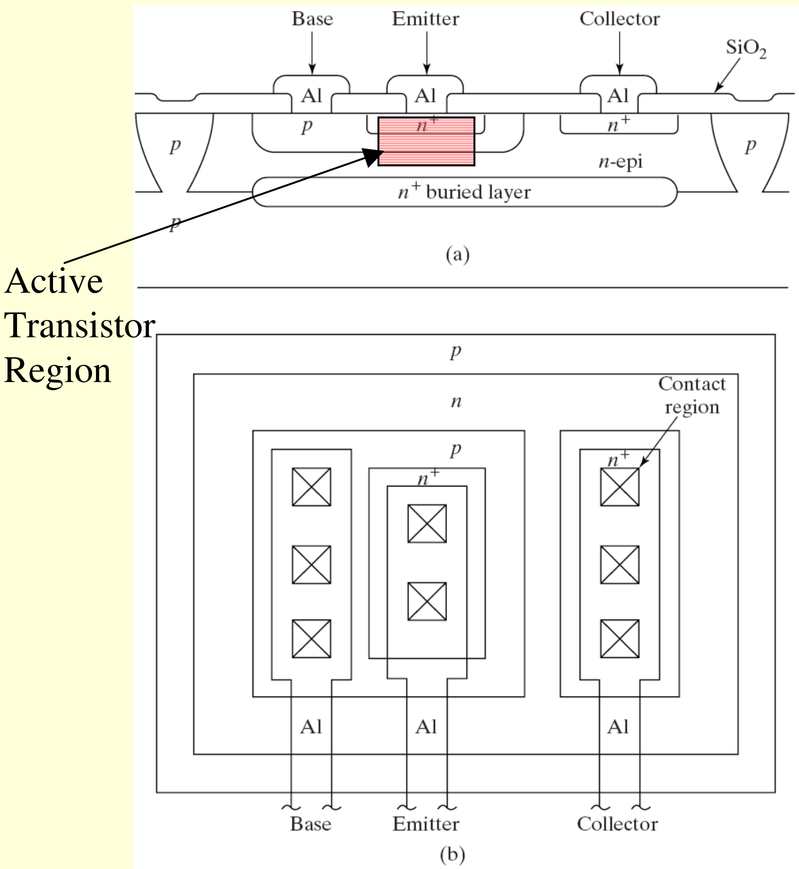


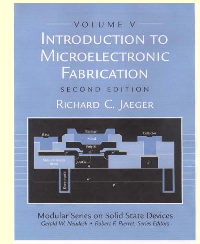
FIGURE 1.5

The basic structure of a junction-isolated bipolar transistor. (a) The vertical cross section through the transistor; (b) a composite top view of the masks used to fabricate the transistor in (a).

- Bipolar Junction Transistor (BJT)
- Standard Buried Collector Process (SBC)
- n- and p-type semiconductor regions
- Thick and thin oxides
- Etching Openings
- Metal (Al) Interconnections

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

SBC Process
Key Steps



- •Oxidation
- •Photolithography
- •Implantation
- •Diffusion
- •Etching
- •Film Deposition

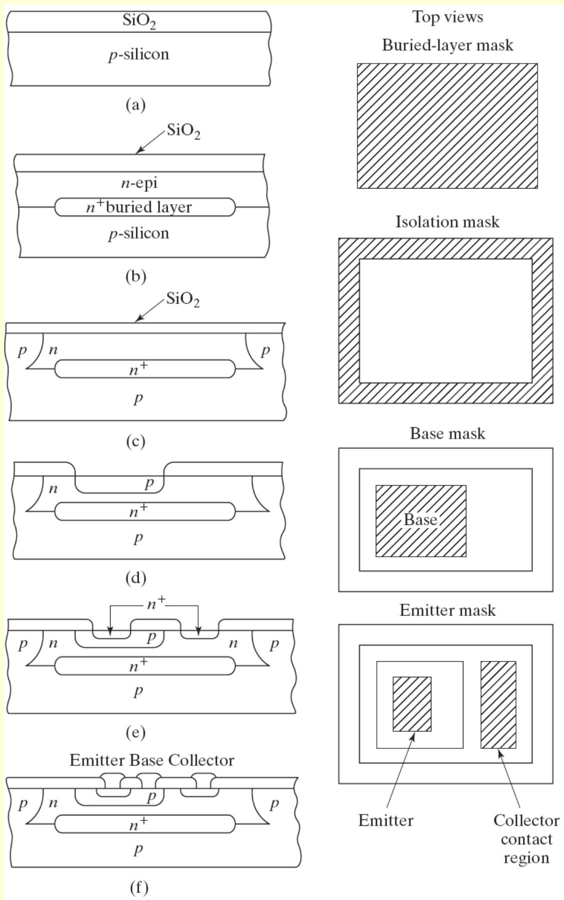
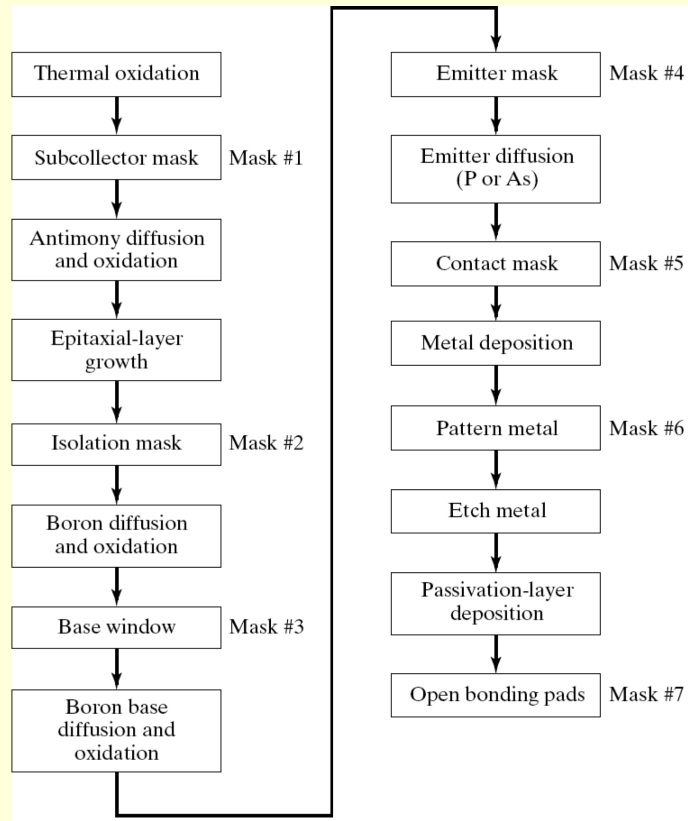


FIGURE 1.9

Cross-sectional view of the major steps in a basic bipolar process. (a) Wafer with silicon dioxide layer; (b) following buried-layer diffusion using first mask, and subsequent epitaxial layer growth and oxidation; (c) following deep-isolation diffusion using second mask; (d) following boron-base diffusion using third mask; (e) fourth mask defines emitter and collector contact regions; (f) final structure following contact and metal mask steps.



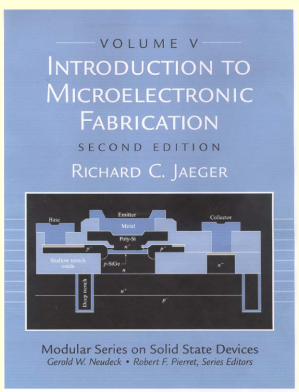
For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Introduction to Microelectronic Fabrication

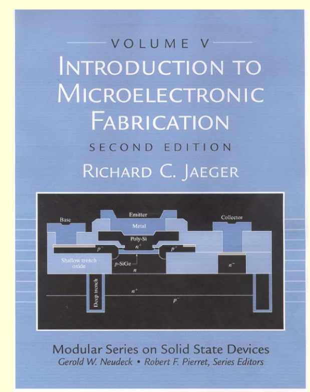
by

Richard C. Jaeger
Distinguished University Professor
ECE Department

Auburn University



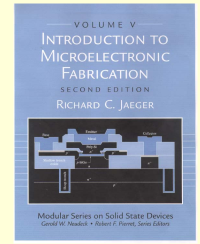
Chapter 9
MOS Process Integration



For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

NMOS Transistors

Structure and Model



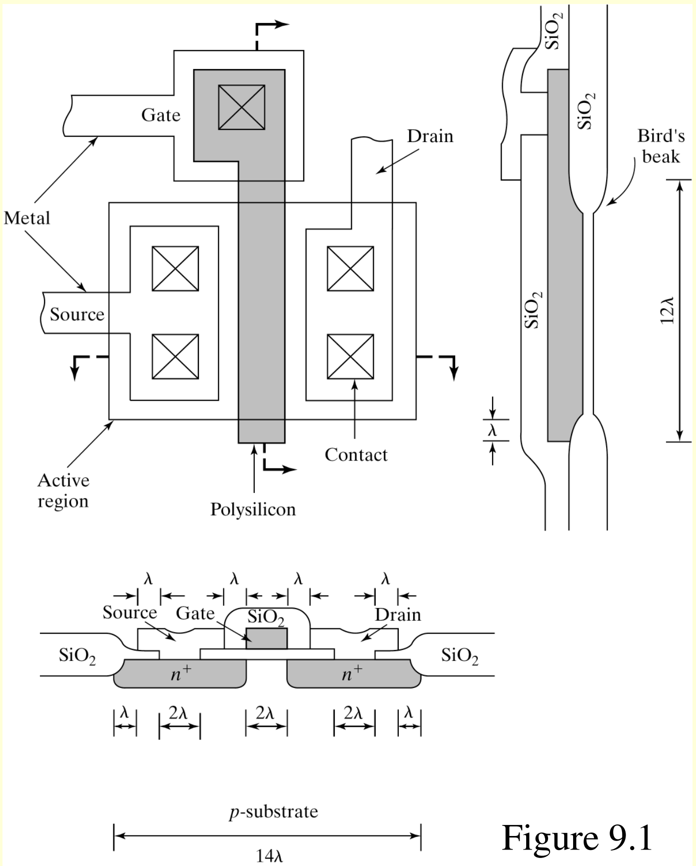
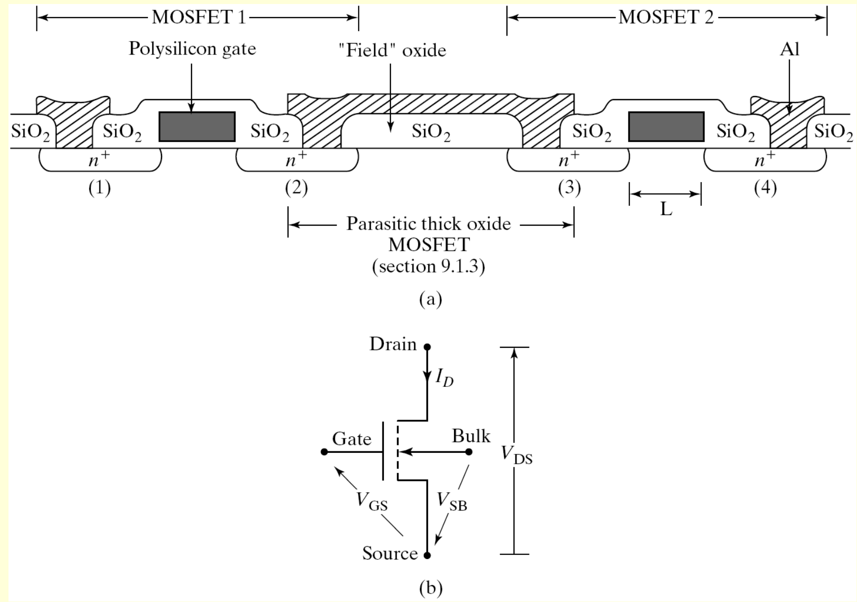


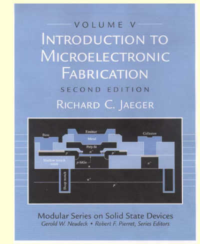
Figure 9.1



$$I_D = K_n'\left(\frac{W}{L}\right)\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS} \qquad K_n' = \mu_n C_O = \mu_n \frac{\varepsilon_{OX}}{X_O}$$

$$V_{GS} > V_{TN} \qquad V_{TN} = \text{threshold voltage}$$

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.



NMOS Transistors

Threshold Voltage

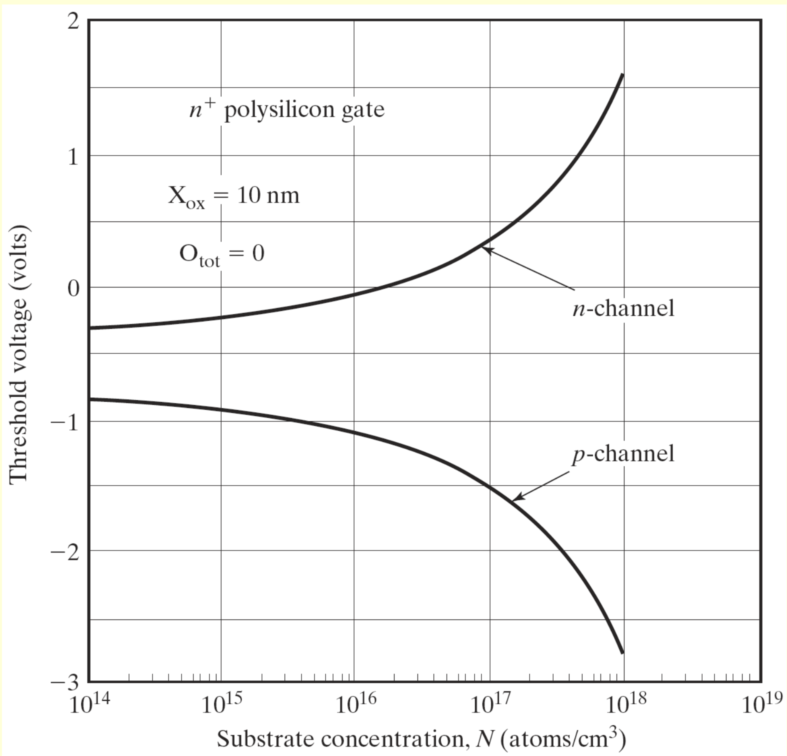


Figure 9.2
Threshold voltage vs. substate doping

$$V_{TN} = \Phi_M - \chi - \frac{E_G}{2q} + |\phi_F| + \frac{\sqrt{2K_S\varepsilon_o q N_B\left(2|\phi_F| + V_{SB}\right)}}{C_O} - \frac{Q_{tot}}{C_O}$$

$$V_{TP} = \Phi_M - \chi - \frac{E_G}{2q} - |\phi_F| - \frac{\sqrt{2K_S\varepsilon_o q N_B\left(2|\phi_F| + V_{SB}\right)}}{C_O} - \frac{Q_{tot}}{C_O}$$

$$\phi_F = \frac{kT}{q}\ln\left(\frac{N_B}{n_i}\right)$$

Φ_M = metal - semiconductor work function

χ = electron affinity

$\Phi_M - \chi = -0.11$ V for aluminum gates

$\Phi_M - \chi = -0$ V for an n^+ polysilicon gate

$\Phi_M - \chi = +1.12$ V (E_G) for a p^+ polysilicon gate

Q_{tot} = total oxide charge

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

NMOS Transistors
Shallow Trench Isolation

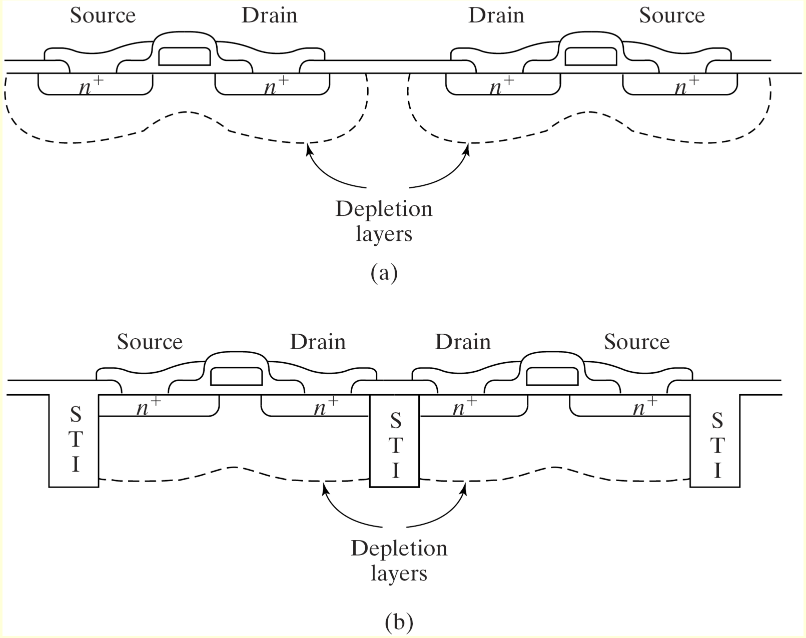
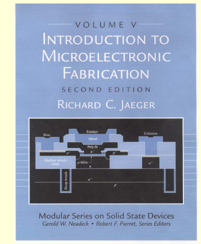


Figure 9.7
Isolation Techniques (a) Intrinsic (b) Shallow trench

- Depletion layers from adjacent devices must not merge
- Shallow trench isolation reduces separation required between devices

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

NMOS Transistors
Depletion Layer Widths



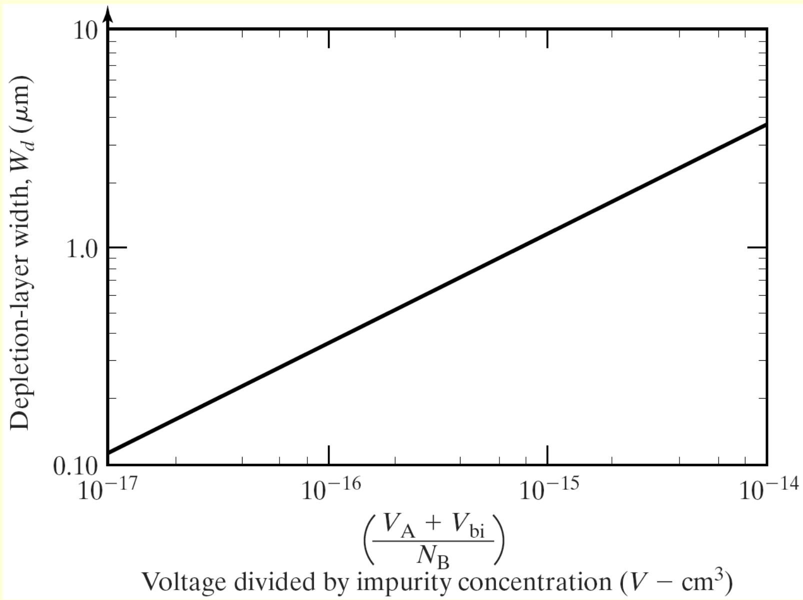


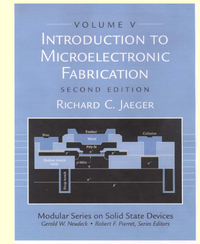
Figure 9.4
Depletion-layer width of a one-sided step junction as a function of doping and applied voltage

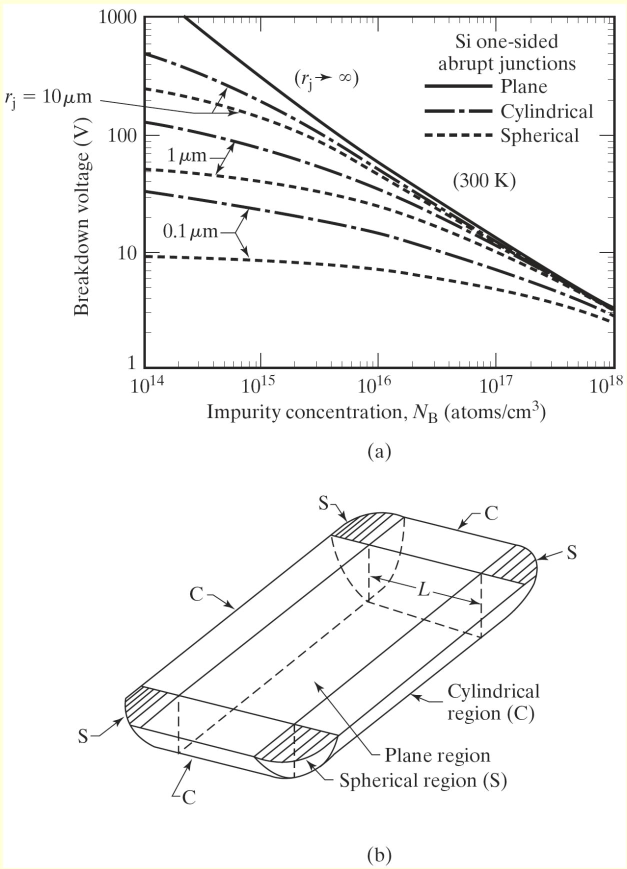
- NMOS transistors are "self isolating"
- However, depletion layer widths limit minimum device separation
- Light doping reduces junction capacitances

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

NMOS Transistors

Junction Breakdown





- Substrate doping must be selected to support required drain-substrate voltage
- Light doping increases breakdown voltage
- Cylindrical and spherical curvatures reduce the breakdown voltage

FIGURE 9.3

(a) Abrupt *pn* junction breakdown voltage versus impurity concentration on the lightly doped side of the side of the junction for both cylindrical and spherical structures. r_j is the radius of curvature. (b) Formation of cylindrical and spherical regions by diffusion through a rectangular window. Copyright 1985, John Wiley & Sons, Inc. Reprinted with permission from Ref. [5].

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

NMOS Transistors
Lightly Doped Drains (LDD)

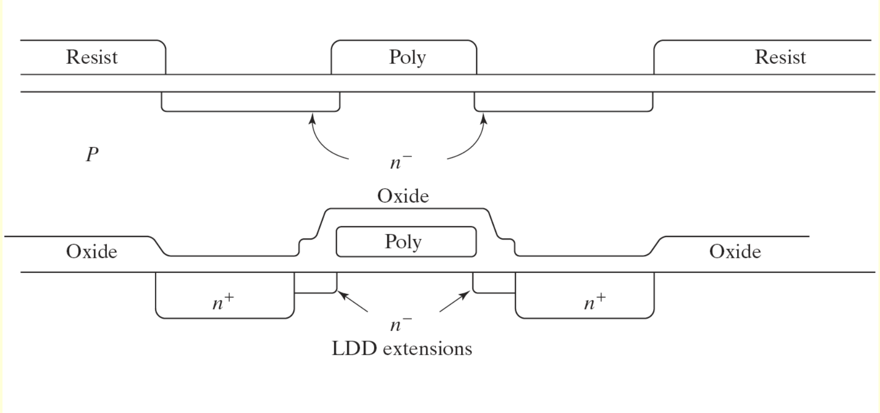


Figure 9.8
Self-aligned polysilicon-gate transistor with lightly doped source/drain regions

- Heavy doping in drain near edge of channel reduces breakdown voltage of the device and reduces reliability
- LDD structure reduce drain doping at edge of channel

MOS Transistor Layout

Alignment Errors

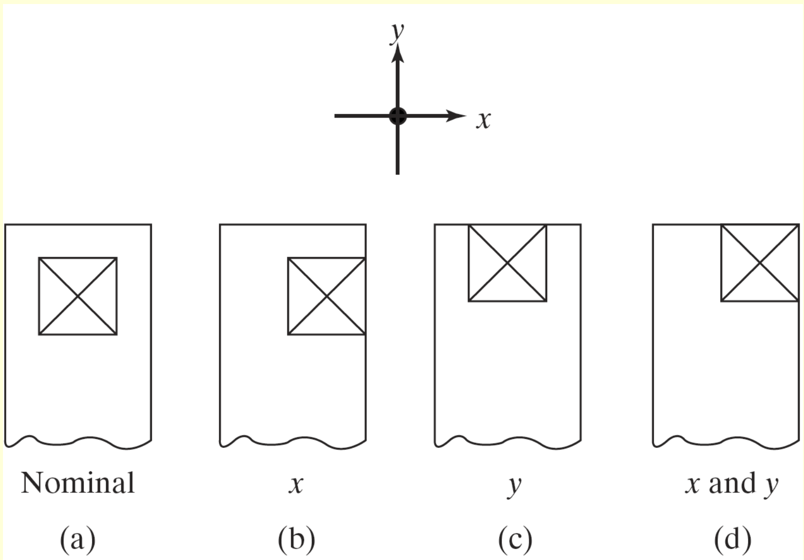
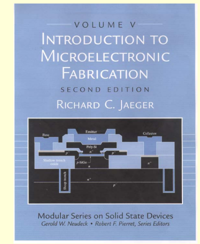


Figure 9.9

- Levels must overlap by at least one alignment tolerance to ensure coverage and proper device operation
- Figure shows various possible misalignments between two levels

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

MOS Transistor Layout
λ-Based Design Rules



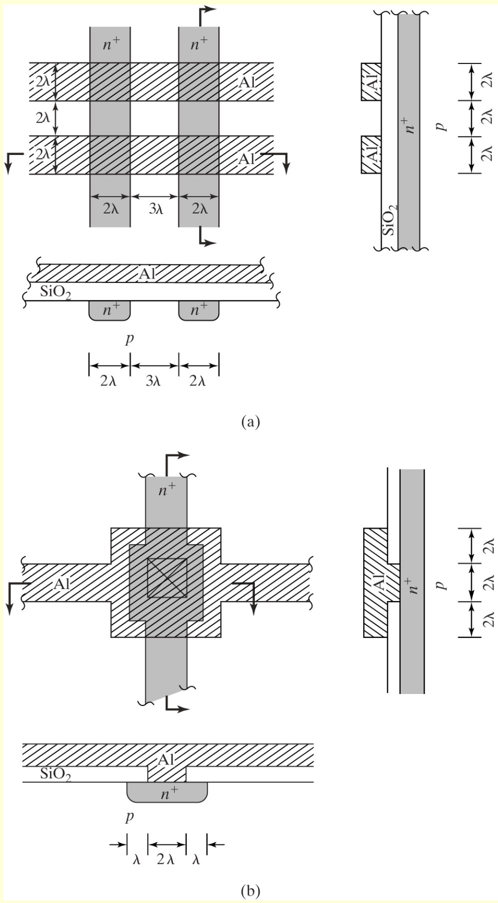


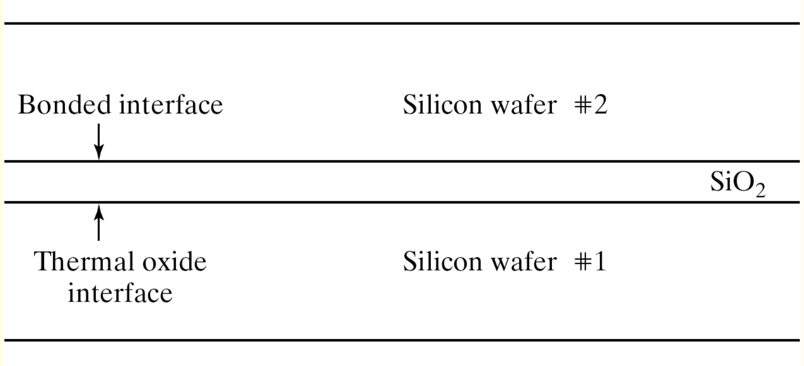
Figure 9.11

- Design rules for previous alignment sequence
- Minimum Feature Size F = 2λ
- Alignment Tolerance T = λ

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

CMOS Technology

Silicon-on-Insulator (SOI)

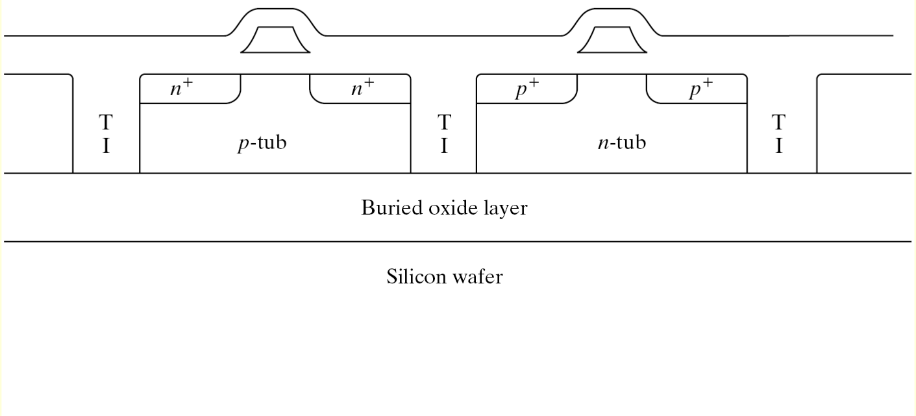


- Two wafers can be bonded together to form silicon on insulator material
- Deep oxygen implantation can be used to create a buried oxide layer (SIMOX)

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

CMOS Technology

Silicon-on-Insulator (SOI)



- Figure 9.20 - Trench isolated SOI
- Silicon on insulator

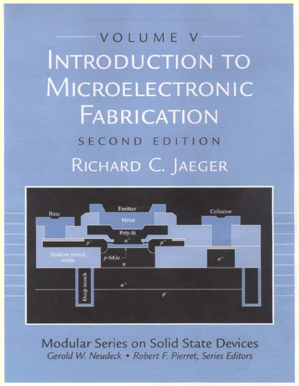
For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Introduction to Microelectronic Fabrication

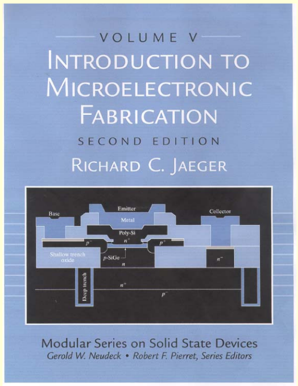
by

Richard C. Jaeger
Distinguished University Professor
ECE Department

Auburn University



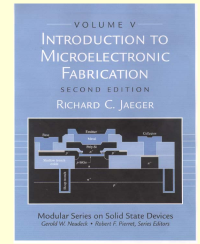
Chapter 10
Bipolar Process Integration

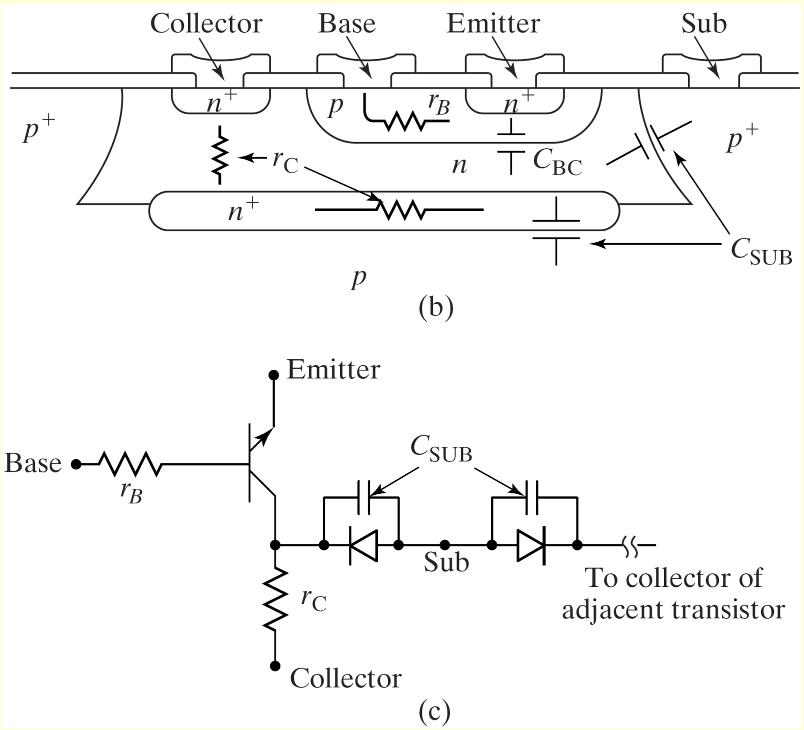


For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Npn Bipolar Transistors

Standard Buried Collector (SBC) Process





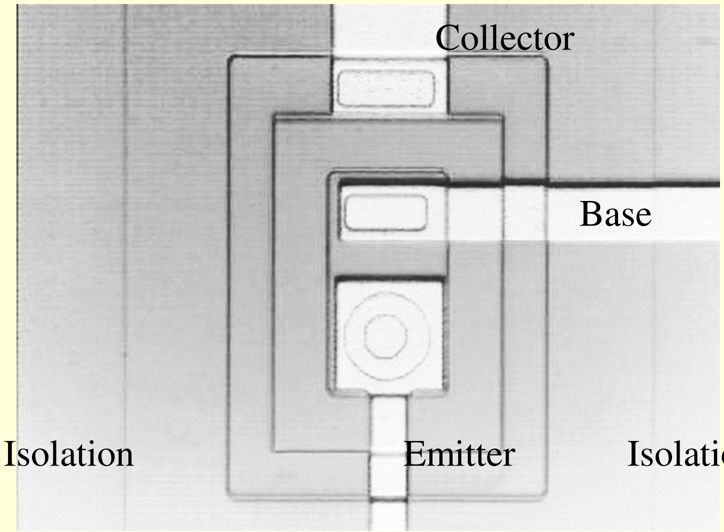


FIGURE 10.1

(a) Photo of an SBC transistor (b) Cross section of a transistor fabricated with the SBC process showing the collector-base capacitances and the base and collector series resistances; (b) lumped circuit model for the transistor showing back-to-back diodes which provide isolation between adjacent transistors.

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Npn Bipolar Transistors
SBC Process

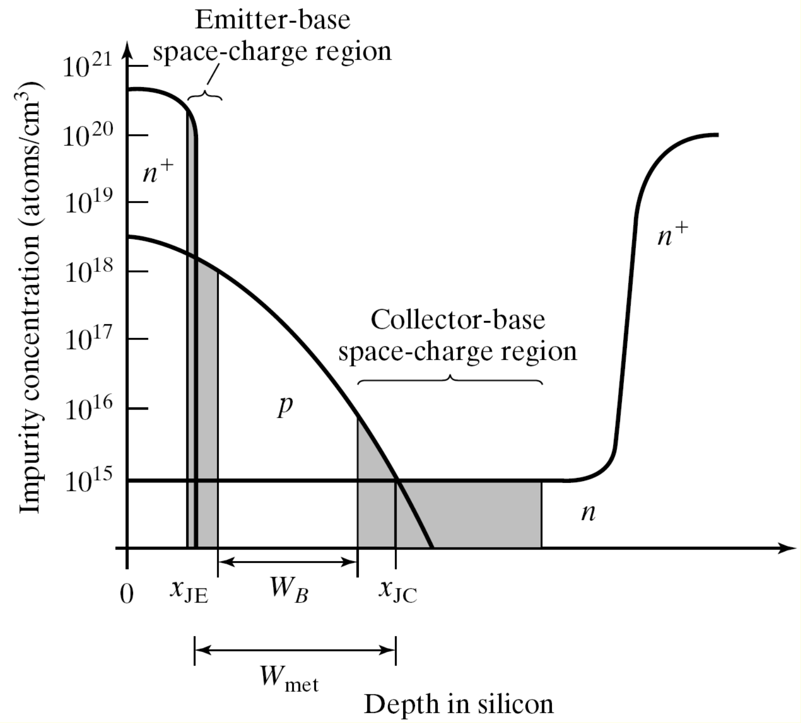


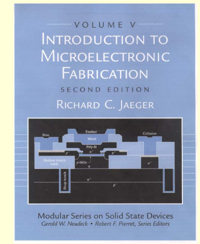
FIGURE 10.2

Vertical impurity profile in typical bipolar junction transistor. The shaded regions represent the emitter-base and collector-base space-charge regions. The metallurgical basewidth and electrical basewidth are indicated by W_{met} and W_B, respectively.

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Npn Bipolar Transistors

Current Gain & Unity Gain Frequency



Current Gain β

$$\beta = \frac{I_C}{I_B}$$

$$\beta^{-1} = \frac{G_B}{G_E} + \frac{W_B^2}{\eta L_B^2}$$

W_B = base width

L_B = diffusion length in the base

G_B and G_E = base and emitter Gummel numbers

$$G_B = \int_{base} \frac{N(x)}{D_B(x)} dx \qquad G_E = \int_{emitter} \frac{N(x)}{D_E(x)} dx$$

Unity Gain Frequency f_T

$$f_T = \frac{1}{2\pi\tau}$$

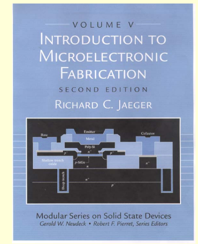
$$\tau = r_E C_{BE} + \frac{W_B^2}{\eta D_B} + (C_{JC} + C_{sub}) r_C + \frac{X_C}{2V_S}$$

τ = transit time

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

SBC Transistor Layout

Design Rules



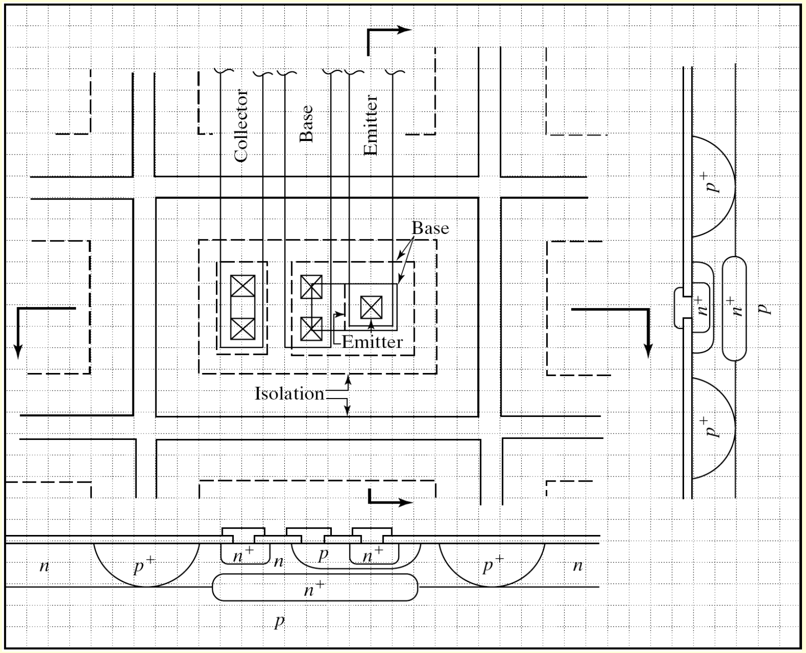


TABLE 10.1 Bipolar Transistor Design Rules for Fig. 10.17.	
Minimum feature size	5 μm
Worst-case alignment tolerance between levels	2 μm
Epitaxial-layer thickness	10 μm
Collector-base junction depth	5 μm
Emitter-base junction depth	3 μm
Minimum emitter-to-collector spacing at surface	5 μm
Minimum base-to-isolation spacing at surface	5 μm
Minimum collector contact n^+ diffusion to isolation spacing	5 μm
Minimum collector contact n^+ diffusion to base spacing	5 μm
Buried-layer diffusion (both up and down)	2 μm
Buried layer to isolation spacing	5 μm
Buried layer pattern slift	10 μm
Lateral diffusion = vertical diffusion	

Figure 10.17
SBC transistor layout using the design rules in Table 10.1

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Advanced Bipolar Devices

Oxide Isolation

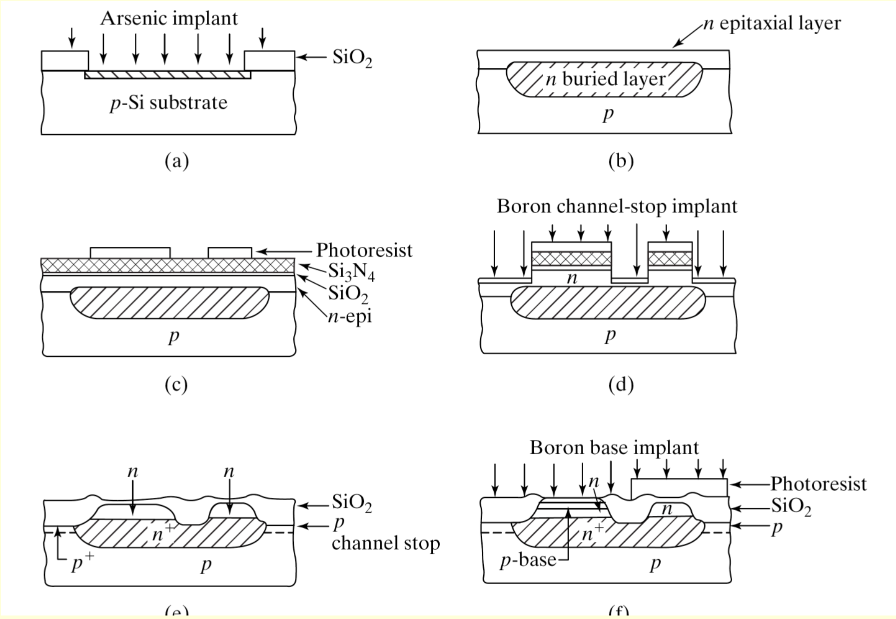
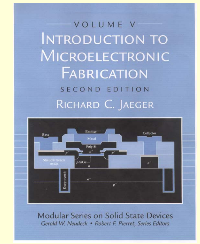


FIGURE 10.18

Process sequence for a high-performace oxide-isolated bipolar transistor. (a) Buried-layer formation; (b) epitaxial layer growth; (c) mask for selective oxidation; (d) boron implant prior to recessed oxide growth; (e) selective oxidation; 9f) base mask and boron base implantation; (g) emitter, base contact, and collector contact mask; (h) p^+ base contact implantation; (i) arsenic implantation for emitter and collector contact; (j) structure completed with multilayer metallization. Copyright 1985, John Wiley & Sons, Inc. Reprinted with permission from Ref. [5].

Advanced Bipolar Devices

Oxide Isolation



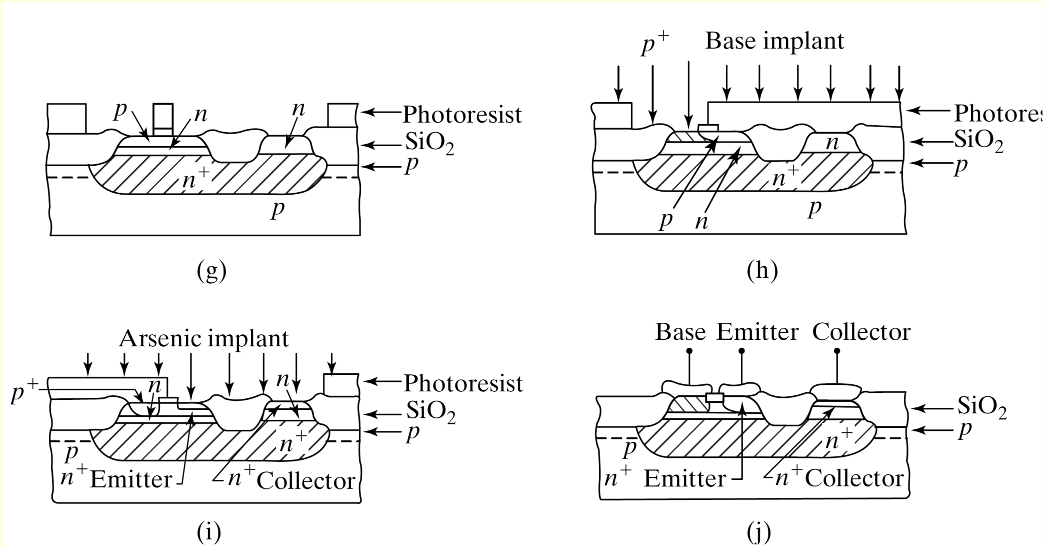


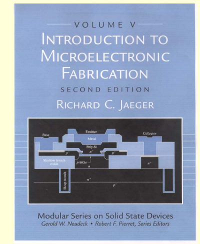
FIGURE 10.18

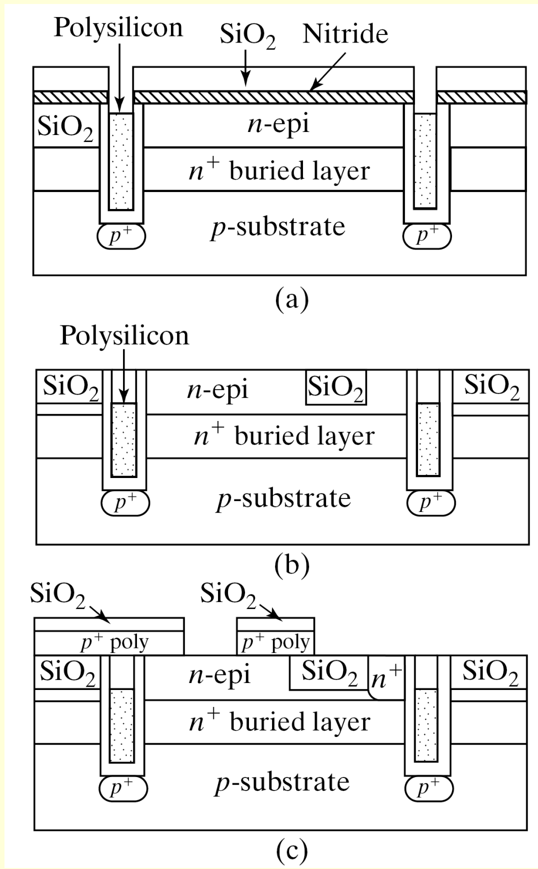
Process sequence for a high-performace oxide-isolated bipolar transistor. (a) Buried-layer formation; (b) epitaxial layer growth; (c) mask for selective oxidation; (d) boron implant prior to recessed oxide growth; (e) selective oxidation; 9f) base mask and boron base implantation; (g) emitter, base contact, and collector contact mask; (h) p^+ base contact implantation; (i) arsenic implantation for emitter and collector contact; (j) structure completed with multilayer metallization. Copyright 1985, John Wiley & Sons, Inc. Reprinted with permission from Ref. [5].

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Advanced Bipolar Devices

Trench Isolation





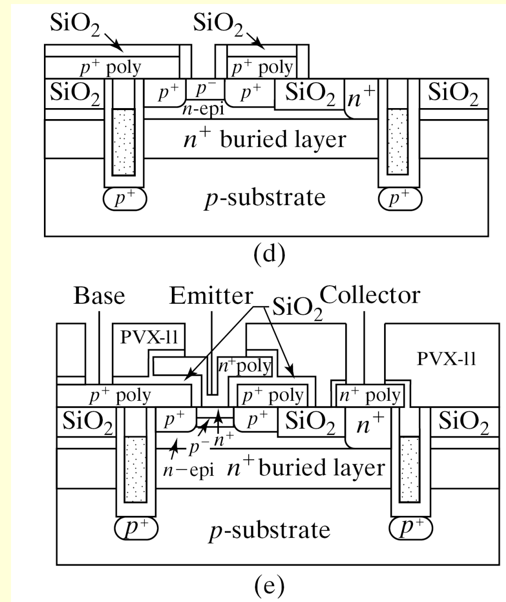


FIGURE 10.19

A high-performance bipolar transistor structure with an f_T of 10 GHz. (a) Isolation is achieved using deep-trench isolation with polysilicon and silicon dioxide refill; (b) structure following selective oxidation; (c) p^+ polysilicon deposited and patterned; (d) diffusion from doped polysilicon forms the extrinsic base region and base contacts; a self-aligned implantation forms the intrinsic base; (e) diffusion from n^+ polysilicon forms the emitter and the emitter and collector contacts of the transistor. Copyright 1997, IEEE. Reprinted with permission from Ref. [8].

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

BiCMOS Processes
CMOS + Bipolar

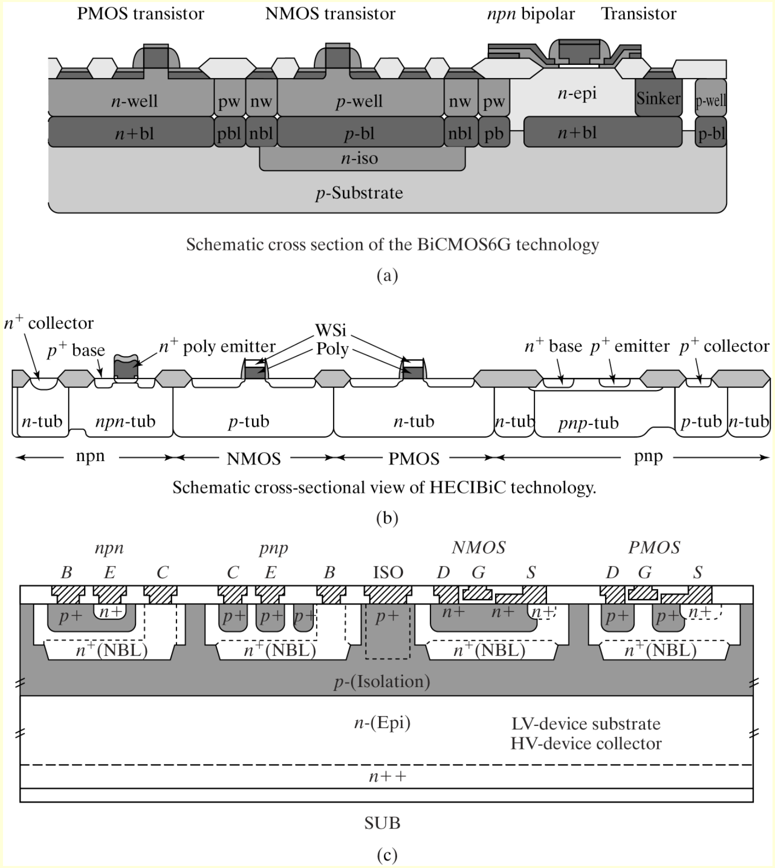
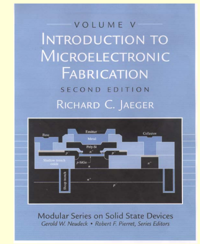


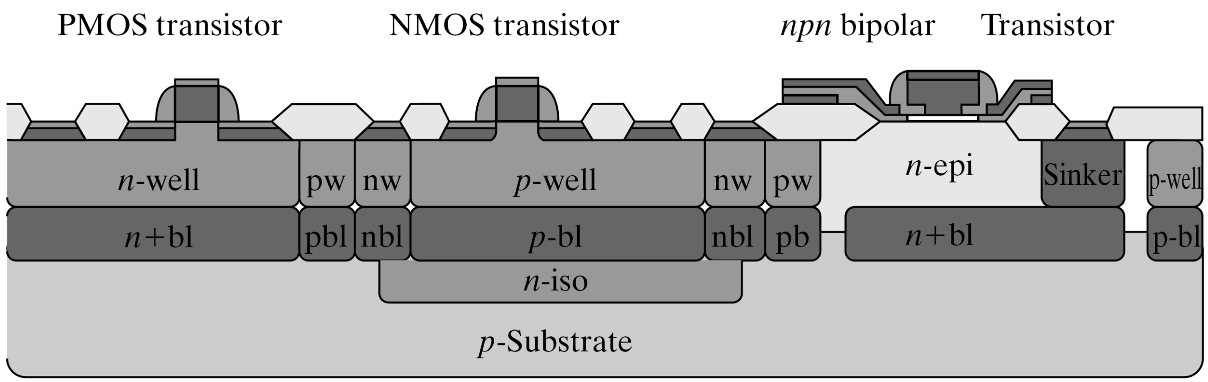
FIGURE 10.25

BiCMOS technology cross sections (a) A dual-well CMOS + npn process. Well formation is preceded by n- and p-type buried layer diffusion. (b) A twin-well process which utilizes high energy implantation to reduce collector resistance of the BJTs. Vertical npn and pnp transistors are available in this process. (c) BiCMOS devices in a process designed for power semiconductor applications. Copyright 1999, 1998, 1997, IEEE. Reprinted with permission from Refs. [15, 16, 17].

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

BiCMOS Processes
CMOS + Bipolar





Schematic cross section of the BiCMOS6G technology

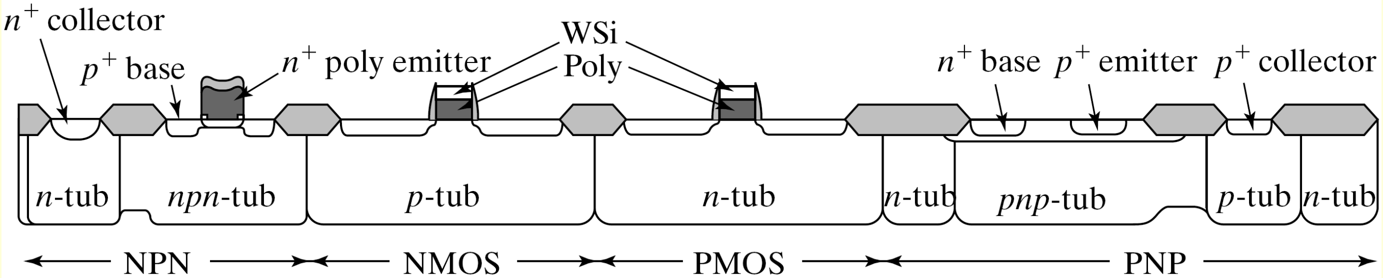
(a)

FIGURE 10.25

BiCMOS technology cross sections (a) A dual-well CMOS + npn process. Well formation is preceded by n- and p-type buried layer diffusion. (b) A twin-well process which utilizes high energy implantation to reduce collector resistance of the BJTs. Vertical npn and pnp transistors are available in this process. (c) BiCMOS devices in a process designed for power semiconductor applications. Copyright 1999, 1998, 1997, IEEE. Reprinted with permission from Refs. [15, 16, 17].

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

BiCMOS Processes
CMOS + Bipolar



Schematic cross-sectional view of HECIBiC technology.

(b)

FIGURE 10.25

BiCMOS technology cross sections (a) A dual-well CMOS + npn process. Well formation is preceded by n- and p-type buried layer diffusion. (b) A twin-well process which utilizes high energy implantation to reduce collector resistance of the BJTs. Vertical npn and pnp transistors are available in this process. (c) BiCMOS devices in a process designed for power semiconductor applications. Copyright 1999, 1998, 1997, IEEE. Reprinted with permission from Refs. [15, 16, 17].

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

BiCMOS Processes

CMOS + Bipolar

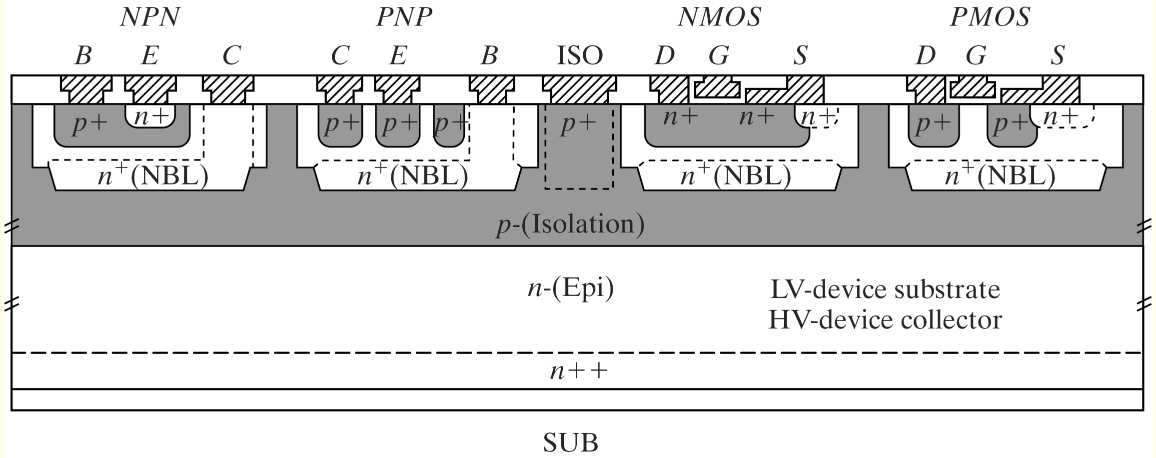


FIGURE 10.25

BiCMOS technology cross sections (a) A dual-well CMOS + npn process. Well formation is preceded by n- and p-type buried layer diffusion. (b) A twin-well process which utilizes high energy implantation to reduce collector resistance of the BJTs. Vertical npn and pnp transistors are available in this process. (c) BiCMOS devices in a process designed for power semiconductor applications. Copyright 1999, 1998, 1997, IEEE. Reprinted with permission from Refs. [15, 16, 17].

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.

Bipolar Process Integration
References

[1] J.G. Fossum, "Computer-Aided Numerical Analysis of Silicon Solar Cells," *Solid-State Electronics, 19*, 269–277 (April, 1976).

[2] H. Lawrence and R.M. Warner, Jr., *Bell System Technical Journal, 39*, 389–403 (March, 1960).

[3] P.R. Wilson, "The Emitter-Base Breakdown Voltage of Planar Transistors," *Solid-State Electronics, 17*, 465–467 (May, 1974).

[4] R.A. Colclaser, *Microelectronics Processing and Device Design*, John Wiley & Sons, New York, 1980.

[5] S.M. Sze, *Semiconductor Devices—Physics and Technology*, John Wiley & Sons, New York, 1985.

[6] R.C. Jaeger, *Microelectronic Circuit Design*, McGraw-Hill Book Company, Burr Ridge, IL: 1997.

[7] **Wilamowski SBD**

[8] M. Vora, Y.L. Ho, S. Bhamre, F. Chien, G. Bakker, H. Hingarh, and C. Schmitz, "A Sub-100 Picosecond Bipolar ECL Technology, *IEEE IEDM Technical Digest*, p. 34–37 (December, 1985).

[9] John D. Cressler, "Re-engineering Silicon: Si-Ge Heterojunction Bipolar Technology," *IEEE Spectrum*, pp. 49–55, March 1995.

[10] E.F. Crabbe et al., "Vertical profile optimzartion of very high frequency epitaxial Si and SiGe-base bipolar transistors," *1993 IEDM Digest*, pp. 83–86., December 1993.

[11] $$$J. Sanders, W.R. Morcom, and C.S. Kim, "An Improved Dielectric-Junction Combination Isolation Technique for Integrated Circuits," *IEEE IEDM Technical Digest*, p. 38–40 (December, 1973).

[12] J. L. Davidson and D. R. Mason, Method of Etching Silicon Crystals, U.S. Patent #3,728,179, issued April 17, 1973.

[13] R. Patel, W. Milam, G. Cooley, M. Corsi, J. Erdeljac and L. Hunter, "A 30 V Complementary Bipolar Technology on SOI for High Speed Precision Analog Circuits," *1997 IEEE BCTM Digest*, pp. 48–51, September 1997.

[14] D. Harame, "High Performance BiCMOS Process Integration Trends, Issues and Future Direction," *1997 IEEE BCTM Digest*, pp. 36–43, September 1997.

[15] A. Monroy et al., BiCMOS6G: A High Performance 0.35 µm SiGe BiCMOS Technology for Wireless Applications," *1999 IEEE BCTM Digest*, pp. 121–134, September 1999.

[16] Y-F Chyan et al., "A 50-GHz 0.25 µm Implanted-Base High-energy Implanted Collector Complementary Modular BiCMOS (HEICBiC) Technology for Low-power Wireless-communication VLSIs," *1998 IEEE BCTM Digest*, pp. 128–131, September 1998.

[17] A. Leone, N. Speciale, S. Graffi, G. Masetti and V. Graziano, "Modeling Parasitic Bipolar Devices in Advanced Smart-power Technologies," *1997 IEEE BCTM Digest*, pp. 127–130, September 1997

[18] B.T. Murphy, V.J. Glinski, P.A. Gary, and R.A. Pederson, "Collector Diffusion Isolated Integrated Circuits," *Proceedings of the IEEE, 57*, 1523–1527 (September, 1969).

[19] C. C. Allen, L. H. Clevenger, and D. C. Gupta, "A Point Contact Method of Evaluating Epitaxial Layer Resistivity," *Journal of the Electrochemical Society*, *113*, 508–510 (May, 1966).

[20] H. F. Wolf, *Silicon Semiconductor Data*, Pergamon Press, Oxford, 1969.

For the exclusive use of adopters of the book Introduction to Microelectronic Fabrication, Second Edition by Richard C. Jaeger. ISBN0-201-44494-1.