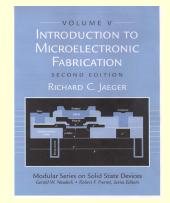
Introduction to Microelectronic Fabrication

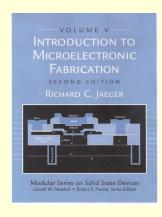
by

Richard C. Jaeger
Distinguished University Professor
ECE Department

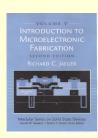
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Chapter 7
Interconnections and Contacts

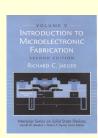


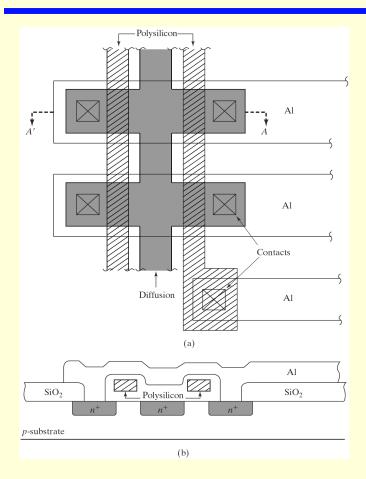
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Interconnections and Contacts MOS Logic Circuit





- 3 Basic Interconnection Levels
 - n⁺ diffusion
 - Polysilicon
 - Aluminum Metallization
- Contacts
 - Al- n^+
 - Al-Polysilicon
 - Al-p
 - Substrate Contact Not Shown

Figure 7.1 Portion of MOS integrated circuit (a) Top view (b) Cross section

Interconnections Resistivity of Metals

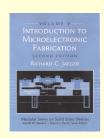


TABLE 7.1 Bulk Resistivity of Metals ($\mu\Omega$ -cm)						
Ag: Silver Al: Aluminum Au: Gold Co: Cobalt Cu: Copper Mo: Molybdenum	1.6 2.65 2.2 6 1.7 5	\$ 438 /lb, Feb 8, 2011 \$ 1.12/lb, Feb 8, 2011 \$ 19898 /lb, Feb 8, 2011 \$ 38 /lb, Feb 8, 2011 \$ 4.4 /lb, Feb 8, 2011				
Ni: Nickel Pd: Paladium Pt: Platinum Ti: Titanium W: Tungsten	7 10 10.6 50 5	\$12 /lb, Feb 8, 2011				

Source: WebElements [http://www.webelements.com]

Hafnium \$ 330 /lb, Feb 8, 2011 Silicon \$.71 /lb, Feb 8, 2011 Commonly Used Metals
Aluminum
Titanium
Tungsten
Copper

Less Frequently Utilized
Nickel
Platinum
Paladium

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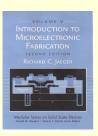
LB KG MT				LME Officials 08 Fe				eb 2011	
USD/LB	Cash	3m	15m		USD/LB	Cash	3m	15m	
Aluminum	1.1431	1.1526	1.1825		Nickel	12.6348	12.6552	12.1495	
Alum Alloy	1.0546	1.0410	1.0092		Lead	1.1648	1.1462	1.1240	
NA Alloy	1.1204	1.1317	1.1521		Tin	14.1748	14.1748	13,9639	
Copper	4.5044	4.5019	4.4067		Zinc	1.1177	1.1265	1.1376	

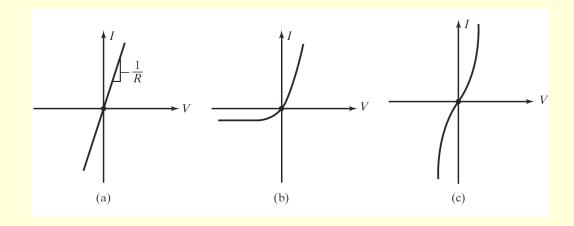
COMEX/NYMEX 9 Feb 2011									
USD/LB	Month	Open	Settle	USD/Troy Oz	Month	Open	Settle		
Copper	Mar 11	4.5920	4.5740y	Gold	Feb 11	1362.80	1363.40y		
Copper	May 11	4.6000	4.5825y	Silver	Mar 11	30.285	30.271y		
Oil/barrel	Apr 11	90.65	90.24y	Platinum	Mar 11	1849.90	1858.50s		
Nat Gas/mmBTU	Apr 11	4.094	4.072y	Palladium	Mar 11	838.05	838.45y		
		y = yes	sterday's sett	le s = today's settle	ß.				



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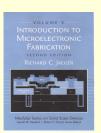
Contacts Ohmic Contact Formation

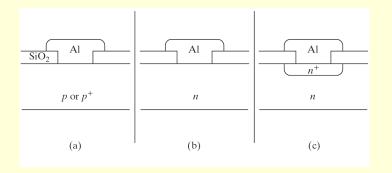




- (a) Ideal Ohmic Contact
- (b) Rectifying Contact (similar to diode)
- (c) Practical Nonlinear "Ohmic" Contact

Contacts Ohmic Contact Formation





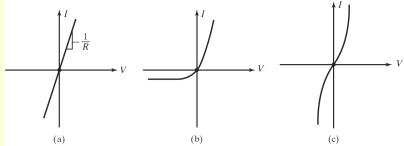


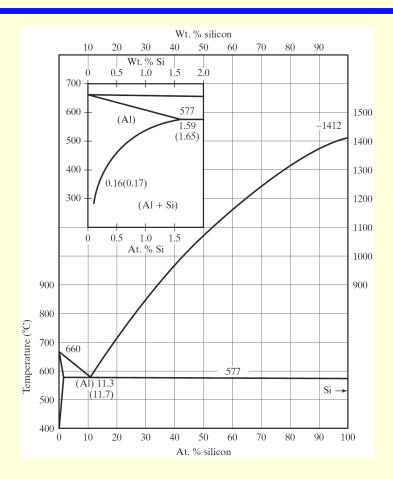
Figure 7.3

Figure 7.2

- Aluminum to p-type silicon forms an ohmic contact similar to Fig. 7.2(a) [Remember Al is p-type dopant]
- Aluminum to n-type silicon can form a rectifying contact (Schottky barrier diode) similar to Fig. 7.3(b)
- Aluminum to n+ silicon yields a contact similar to Fig. 7.3c

Contacts Aluminum-Silicon Phase Diagram





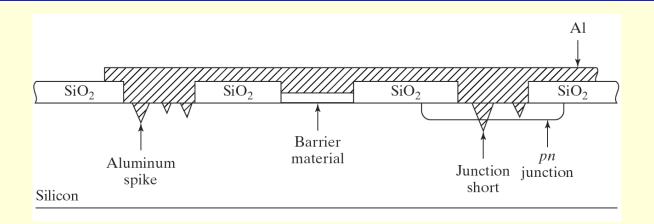
Aluminum-Silicon Eutectic Point 577° C

FIGURE 7.4

Phase diagram of the aluminum-silicon system. The silicon-aluminum eutectic point occurs at a temperature of 577 °C. At contact-alloying temperatures between 450 and 500 °C, aluminum will absorb from 0.5 to 1% silicon. Copyright 1958 McGraw-Hill Book Company, with permission from Ref. [1].

Contacts

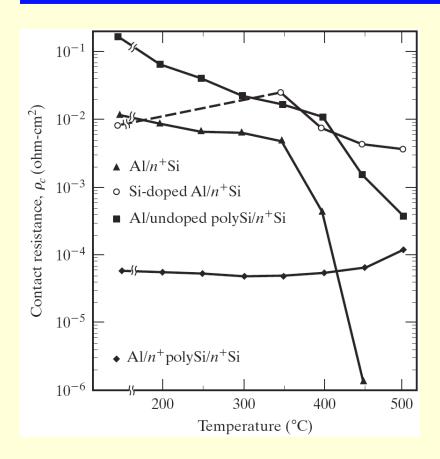
Aluminum Spiking and Junction Penetration



- Silicon absorption into the aluminum results in aluminum spikes
- Spikes can short junctions or cause excess leakage
- Barrier metal deposited prior to metallization
- Sputter deposition of Al 1% Si

Contacts Alloying of Contacts





Alloy to Obtain Very Low Contact Resistivity

Specific Contact Resistivity

$$\rho_c = 1.2 \times 10^{-6} \Omega - cm^2$$

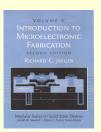
Contact Resistance R_C

$$R_C = \frac{\rho_c}{A}$$
 A = contact area

FIGURE 7.6

Contact resistivity of a variety of aluminum-silicon systems. An alloying temperature of 450 °C is typically used to obtain low-contact resistance for Al-Si contacts. Reprinted with permission from *Solid-State Electronics*, Vol. 23, p. 255-262, M. Finetti et al., "Aluminum-Silicon Ohmic Contact on Shallow n⁺/p Junctions" [2]. Copyright 1980, Pergamon Press, Ltd.

Contacts Contact Resistance



Example for $\rho_{\rm C} = 1 \,\mu\Omega - cm^2$

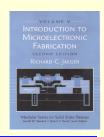
$$A = 10 \mu m \times 10 \mu m = 10^{-6} cm^2$$

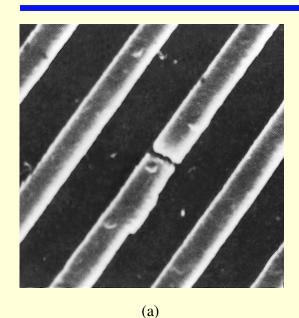
$$R_C = \frac{\rho_C}{A} = 1 \Omega$$

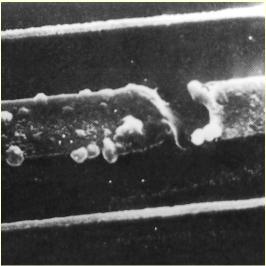
A = 1
$$\mu$$
m x 1 μ m = 10⁻⁸ cm²
 $R_C = 100 \Omega$

A = 0.1
$$\mu$$
m x 0.1 μ m = 10^{-10} cm²
 $R_C = 10 k\Omega$ Unacceptable!

Interconnections Electromigration







(b)

High current density causes voids to form in interconnections

"Electron wind" causes movement of metal atoms

FIGURE 7.7

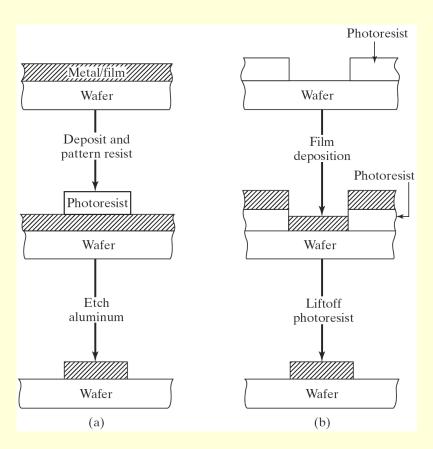
Scanning electron micrographs of aluminum interconnection failure caused by electro-migration. (a) Sputtered aluminum with 0.5% copper; (b) evaporated aluminum with 0.5% copper. Copyright 1980, IEEE. Reprinted with permission from Ref. [3].

$$J = \frac{1A}{(1\mu m)^2} = \frac{10mA}{(10^{-4}cm)^2} = 1 MA/cm^2$$

High Current Densities

Interconnections Liftoff Process

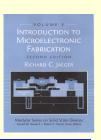




- (a) Subtractive etching process
- (b) Additive metal liftoff process

Figure 7.15

Multilevel Metallization



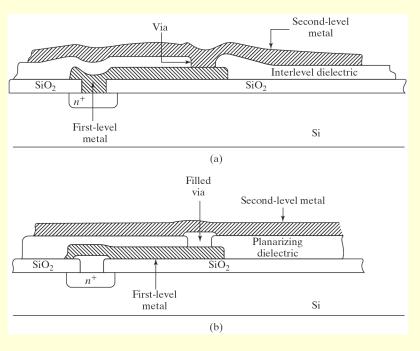
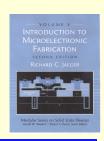


Figure 7.16

- Two level metal processes
- Silicon dioxide, polyimide or silicon nitride dielectrics
- Vias formed to connect between metal levels
- Vias can be filled (b)to improve planarization

Multilevel Metallization



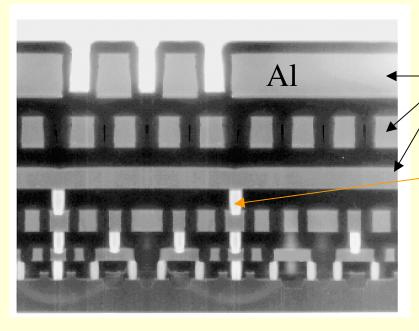
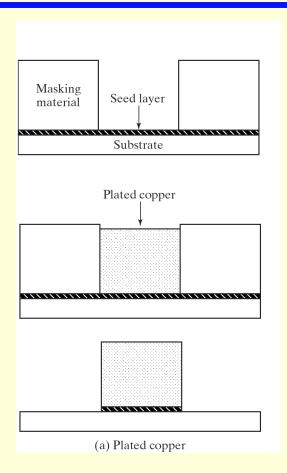


Figure 7.17 Multilevel aluminum metallization with tungsten plugs. Copyright 1998 IEEE. Reprinted with permission from Ref. [7].

- Example of multilevel
 aluminum
 metallization with
 tungsten via plugs
- Planarity achieved through Chemical Mechanical Polishing (CMP)

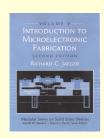
Plated Copper

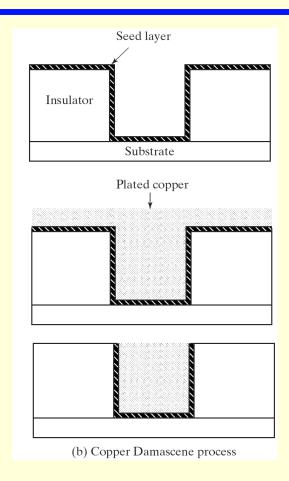




- Copper deposited using "standard" plating processes adapted to microelectronics
- Seed layer deposited
- Mask layer deposited and patterned
- Copper plated up
- Mask layer removed
- Seed layer etched away

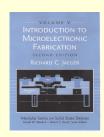
Copper Damascene Process





- Damascene process used to obtain highly planar surfaces
- Dielectric layer (insulator) deposited and patterned
- Seed layer deposited
- Copper plated
- Surface polished mechanical & chemical

Dual Damascene Process



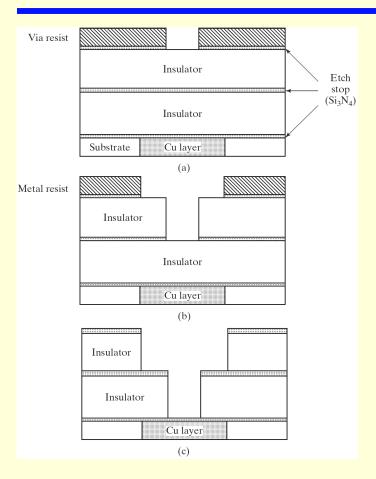


FIGURE 7.19

Dual damescene process flow. (a) An insulator sandwich is first deposited and the upper nitride layer is patterned. The insulator layer is etched. The etch terminates on the silicon nitride etch stop. (b) The nitride layer is patterned and etched. (c) Following the next oxide etch step, two different width openings exist in the two oxide layers. (d) Barrier and seed layers are deposited and plated with copper (e) Final structure following removal of excess copper.

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Dual Damascene Process (cont.)



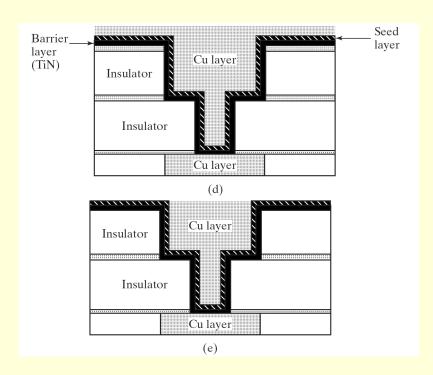
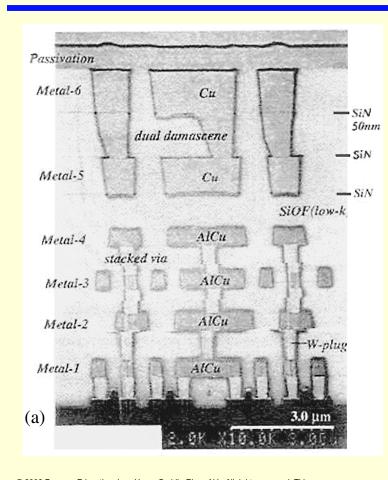


FIGURE 7.19

Dual damescene process flow. (a) An insulator sandwich is first deposited and the upper nitride layer is patterned. The insulator layer is etched. The etch terminates on the silicon nitride etch stop. (b) The nitride layer is patterned and etched. (c) Following the next oxide etch step, two different width openings exist in the two oxide layers. (d) Barrier and seed layers are deposited and plated with copper (e) Final structure following removal of excess copper.

Multilevel Metallization Examples





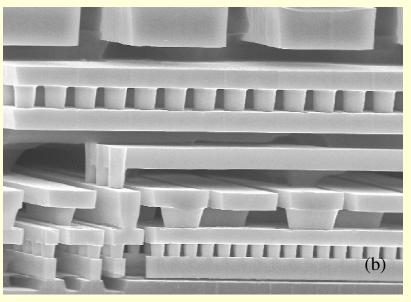
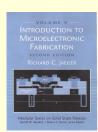


Figure 7.20

(a) Dual Damascene copper combined with aluminum-copper and tungsten plugs on the lower levels. Copyright 1997 IEEE. Reprinted with permission from Ref. [6]. (b) Dual Damsascene Copper. Courtesy of Motorola Inc. Note planarity of both structures.

Interconnections and Contacts References



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End of Chapter 7