Video Article

Fabrication of Flexible Image Sensor Based on Lateral NIPIN Phototransistors

Hyun Myung Kim*[1], Gil Ju Lee*[1], Min Seok Kim[1], Young Min Song[1]

[1]School of Electrical Engineering and Computer Science, Gwangju Institute of Science and Technology

*These authors contributed equally

Correspondence to: Young Min Song at ymsong@gist.ac.kr

URL: https://www.jove.com/video/57502
DOI: doi:10.3791/57502

Keywords: Engineering, Issue 136, lateral phototransistors, flexible electronics, stretchable devices, wearable devices, curved image sensors

Date Published: 6/23/2018

Citation: Kim, H.M., Lee, G.J., Kim, M.S., Song, Y.M. Fabrication of Flexible Image Sensor Based on Lateral NIPIN Phototransistors. *J. Vis. Exp.* (136), e57502, doi:10.3791/57502 (2018).

Abstract

Flexible photodetectors have been intensely studied for the use of curved image sensors, which are a crucial component in bio-inspired imaging systems, but several challenging points remain, such as a low absorption efficiency due to a thin active layer and low flexibility. We present an advanced method to fabricate a flexible phototransistor array with an improved electrical performance. The outstanding electrical performance is driven by a low dark current owing to deep impurity doping. Stretchable and flexible metal interconnectors simultaneously offer electrical and mechanical stabilities in a highly deformed state. The protocol explicitly describes the fabrication process of the phototransistor using a thin silicon membrane. By measuring I-V characteristics of the completed device in deformed states, we demonstrate that this approach improves the mechanical and electrical stabilities of the phototransistor array. We expect that this approach to a flexible phototransistor can be widely used for the applications of not only next-generation imaging systems/optoelectronics but also wearable devices such as tactile/pressure/temperature sensors and health monitors.

Video Link

The video component of this article can be found at https://www.jove.com/video/57502/

Introduction

Bio-inspired imaging systems can provide many advantages compared to the conventional imaging systems[1,2,3,4,5]. Retina or hemispherical ommatidia is a substantial component of biological visual system[1,2,6]. A curved image sensor, which mimics the critical element of animal eyes, can provide a compact and simple configuration of optical systems with low aberrations[7]. Diverse advancements of fabrication techniques and materials, for example, the use of intrinsically soft materials such as organic/nanomaterials[8,9,10,11,12] and the introduction of deformable structures to semiconductors including silicon (Si) and germanium (Ge)[1,2,3,13,14,15,16,17], realize the curved image sensors. Among them, Si-based approaches provide inherent advantages such as an abundance of material, mature technology, stability, and optical/electrical superiority. For this reason, although Si has intrinsic rigidity and brittleness, Si-based flexible electronics have been widely studied for various applications, such as flexible optoelectronics[18,19,20] including curved image sensors[1,2,3], and even wearable healthcare devices[21,22].

In a recent study, we analyzed and improved the electrical performance of a thin Si photodetector array[23]. In that study, the optimum single unit cell of the curved photodetector array is a phototransistor (PTR) type that consists of a photodiode and blocking diode. The base junction gain amplifies a generated photocurrent, and hence it exhibits a route to improve an electrical performance with a thin film structure. In addition to the single cell, the thin film structure is suitable to suppress a dark current, which is considered as noise in the photodetector. Regarding doping concentration, a concentration larger than 10^{15} cm^{-3} is sufficient to achieve an exceptional performance in which the diode characteristics can be maintained with a light intensity over 10^{-3} W/cm^2 [23]. Moreover, the PTR single cell has a low column noise and optically/electrically stable properties compared to that of the photodiode. Based on these design rules, we fabricated a flexible photodetector array that consists of thin Si PTRs using a silicon-on-insulator (SOI) wafer. In general, an important design rule of flexible image sensors is the neutral mechanical plane concept which defines the position through the thickness of the structure where strains are zero for an arbitrarily small r[24]. Another crucial point is a serpentine geometry of the electrode because a wavy shape provides fully reversible stretchability to the electrode. Due to these two important design concepts, the photodetector array can be flexible and stretchable. It facilitates the 3D deformation of the photodetector array into a hemispherical shape or a curved shape like the retina of animal eyes[2].

In this work, we detail the processes for the fabrication of the curved PTR array using semiconductor fabrication processes (*e.g.*, doping, etching, and deposition) and transfer printing. Also, we characterize a single PTR in terms of an I-V curve. In addition to the fabrication method and individual cell analysis, the electrical feature of the PTR array is analyzed in deformed states.

Protocol

CAUTION: Some chemicals (*i.e.*, hydrofluoric acid, buffered oxide etchant, isopropyl alcohol, *etc.*) used in this protocol can be hazardous to health. Please consult all relevant material safety data sheets before any sample preparation takes place. Utilize appropriate personal protective equipment (*e.g.*, lab coats, safety glasses, gloves) and engineering controls (*e.g.*, wet station, fume hood) when handling etchants and solvents.

1. Si Doping and Isolation

NOTE: See **Figure 1a** - **1d**.

1. Prepare a doped SOI wafer by ion implantation with the conditions as follows: dopant-phosphorous/boron, energy of 80/50 keV, and a dose of 5 x 10^{15}/3 x 10^{15} cm^{-3} for n^+ and p^+ doping, respectively. To recover a crystallinity of the wafer, anneal the sample at a temperature of 1,000 °C for 120 min in a furnace after ion implantation. Prepare the doped samples by using the ion implantation process from the National NanoFab Center (NNFC) for high process stability and deep doping depth (**Figure 1a**).
2. To remove the native oxide, dip the diced sample using a Teflon dipper in buffered oxide etchant (BOE) for 5 s and clean the diced sample sequentially with acetone, isopropyl alcohol (IPA), and deionized (DI) water.
3. Form a photoresist (PR) pattern for the Si isolation (**Figure 1b**).
    1. Spin coat positive PR on the sample at 4,000 rpm for 40 s and soft bake the coated sample at 90 °C for 90 s. Expose the sample to UV light with a photolithography mask for 10 s.
    2. Immerse the sample in the developer for 1 min to define the pattern, clean it in DI water, and dry it with an N_2 blowgun while holding it with forceps. Hard bake the sample for hardening the PR layer at 110 °C for 5 min.
4. Dry etch the sample of Si using inductively coupled plasma-reactive ion etching (ICP-RIE) with 100 W RF power, 0 W ICP power, 30 mTorr chamber pressure, and SF_6 gas (40 sccm) for 6 min (**Figure 1c**).
5. To remove a buried oxide layer, dip the samples in hydrofluoric acid 49% for 2 min, using a Teflon dipper (**Figure 1d**).
6. Clean the sample sequentially with acetone, IPA, and DI water. To remove the moisture, dry the sample with an N_2 blowgun while holding it with forceps.

2. Sacrificial Oxide Layer Deposition

NOTE: See **Figure 1e** - **1g**.

1. Deposit a SiO_2 sacrificial layer with a thickness of 130 nm using plasma enhanced chemical vapor deposition (PECVD) with a temperature of 230 °C, 20 W RF power, 1000 mTorr pressure, SiH_4 gas (100 sccm), and N_2O gas (800 sccm) for 2 min (**Figure 1e**).
2. Pattern the PR layer as a mask for a SiO_2 sacrificial layer (**Figure 1f**).
    1. Spin coat positive PR on the sample at 4,000 rpm for 40 s and soft bake the coated sample at 90 °C for 90 s. Expose the sample to UV light with a photolithography mask for 10 s.
    2. Immerse the sample in the developer for 1 min to define the pattern, clean it in DI water, and dry it with N_2 blowgun while holding it with forceps. Hard bake the sample for hardening the PR layer at 110 °C for 5 min.
3. To pattern the PECVD oxide layer, dip the sample in BOE for 30 s, using a Teflon dipper (**Figure 1g**).
4. Clean the sample sequentially with acetone, IPA, and DI water. To remove the moisture, dry the sample with an N_2 blowgun while holding it with forceps.

3. Deposition of the First Layer of Polyimide and Performing the First Metallization

1. Spin coat polyimide (PI) on the sample at 4,000 rpm for 60 s, anneal it at 110 °C for 3 min and at 150 °C for 10 min on a hot plate, and anneal it at 230 °C for 60 min in an N_2 atmosphere by supplying N_2 to the oven (**Figure 1h**).
2. Deposit a SiO_2 layer with a thickness of 130 nm by using PECVD with a temperature of 230 °C, 20 W RF power, 1,000 mTorr pressure, SiH_4 gas (100 sccm), and N_2O gas (800 sccm) for 2 min.
3. Pattern the SiO_2 as a hard mask layer for PI dry etching (**Figure 1i**).
    1. Spin coat positive PR on the sample at 4,000 rpm for 40 s and soft bake the coated sample at 90 °C for 90 s. Expose the sample to UV light with a photolithography mask for 10 s.
    2. Immerse the sample in the developer for 1 min to define the pattern, clean it in DI water, and dry it with an N_2 blowgun while holding it with forceps. Hard bake the sample for hardening the PR layer at 110 °C for 5 min.
    3. To pattern the SiO_2 hard mask, dip the sample in BOE for 30 s using a Teflon dipper, clean it in DI water, and dry it with an N_2 blowgun while holding it with forceps.
4. Dry etch the PI by using RIE with 30 W RF power, O_2 gas (30 sccm), and Ar gas (70 sccm) for 20 min.
5. To remove the PECVD oxide layer, dip the sample in BOE for 30 s, using a Teflon dipper.
6. Clean the sample sequentially with acetone, IPA, and DI water. To remove the moisture, dry the sample with an N_2 blowgun while holding it with forceps.
7. Deposit 10 nm/200 nm thickness of Cr/Au by sputtering.
8. Pattern the Cr/Au metal layer (**Figure 1j**).
    1. Spin coat positive PR on the sample at 4,000 rpm for 40 s and soft bake the coated sample at 90 °C for 90 s. Expose the sample to UV light with a photolithography mask for 10 s.

2. Immerse the sample in the developer for 1 min to define the pattern, clean it in DI water, and dry it with an N_2 blowgun while holding it with forceps. To harden the PR, hard bake the sample at 110 °C for 5 min.
3. Etch the Cr/Au layer with a wet etchant for 60 s/20 s, respectively.

9. Clean the sample sequentially with acetone, IPA, and DI water. To remove the moisture, dry the sample with an N_2 blowgun while holding it with forceps.
NOTE: The cleaning process has to be very careful since there is a risk of peeling the PI layer.

4. Deposition of the Second Layer of Polyimide and Performing the Second Metallization

1. Spin coat PI on the sample at 4,000 rpm for 60 s, anneal it at 110 °C for 3 min and at 150 °C for 10 min on a hot plate, and anneal it at 230 °C for 60 min in an N_2 atmosphere by supplying N_2 to the oven (**Figure 1k**).
2. Deposit a SiO_2 layer with a thickness of 130 nm using PECVD with a temperature of 230 °C, 20 W RF power, 1,000 mTorr pressure, SiH_4 gas (100 sccm), and N_2O gas (800 sccm) for 2 min.
3. Pattern the SiO_2 as a hard mask layer for dry etching (**Figure 1l**).
    1. Spin coat positive PR on the sample at 4,000 rpm for 40 s and soft bake the coated sample at 90 °C for 90 s. Expose the sample to UV light with a photolithography mask for 10 s.
    2. Immerse the sample in the developer for 1 min to define the pattern, clean it in DI water, and dry it with an N_2 blowgun while holding it with forceps. Hard bake the sample for hardening the PR layer at 110 °C for 5 min.
    3. To pattern the SiO_2 hard mask, dip the sample in BOE for 30 s using a Teflon dipper, clean it in DI water, and dry it with an N_2 blowgun while holding it with forceps.

4. Dry etch the PI using RIE with 30 W RF power, O_2 gas (30 sccm), and Ar gas (70 sccm) for 50 min.
5. To remove the PECVD oxide layer, dip the sample in BOE for 30 s, using a Teflon dipper.
6. Clean the sample sequentially with acetone, IPA, and DI water.
7. Deposit 10 nm/200 nm thickness of Cr/Au by sputter coating.
8. Pattern the Cr/Au metal layer (**Figure 1m**).
    1. Spin coat positive PR on the sample at 4,000 rpm for 40 s and soft bake the coated sample at 90 °C for 90 s. Expose the sample to UV light with a photolithography mask for 10 s.
    2. Immerse the sample in the developer for 1 min to define the pattern, clean it in DI water, and dry it with an N_2 blowgun while holding it with forceps. Hard bake the sample for hardening the PR layer at 110 °C for 5 min.
    3. Etch the Cr/Au layer by a wet etchant for 60 s/20 s, respectively.

9. Clean the sample sequentially with acetone, IPA, and DI water.
10. To remove the moisture, dry the clean substrate with a nitrogen blowgun while holding it with forceps.
NOTE: There is a risk of peeling the polyimide layer, so perform the cleaning process very carefully.

5. Encapsulating the Sample with PI and Opening Via Holes and Mesh Structure

1. Spin coat PI on the sample at 4,000 rpm for 60 s, anneal it at 110 °C for 3 min and at 150 °C for 10 min on a hot plate, and anneal it at 230 °C for 60 min in an N_2 atmosphere by supplying N_2 to the oven (**Figure 1n**).
2. Deposit a SiO_2 layer with a thickness of 650 nm using PECVD with a temperature of 230 °C, 20 W RF power, 1,000 mTorr pressure, SiH_4 gas (100 sccm), and N_2O gas (800 sccm) for 8 min.
3. Pattern the SiO_2 as a hard mask layer for dry etching.
    1. Spin coat positive PR on the sample at 4,000 rpm for 40 s and soft bake the coated sample at 90 °C for 90 s. Expose the sample to UV light with a photolithography mask for 10 s.
    2. Immerse the sample in the developer for 2 min to define the pattern, clean it in DI water, and dry it with an N_2 blowgun while holding it with forceps. Hard bake the sample for hardening the PR layer at 110 °C for 5 min.
    3. To pattern the SiO_2 hard mask, dip the sample in BOE for 1 min 30 s using a Teflon dipper, clean it in DI water, and dry it with an N_2 blowgun while holding it with forceps.
    NOTE: Due to the small size of the patterning, it is necessary to let it develop longer than the previous development time.

4. Dry etch the PI using RIE with 30 W RF power, O_2 gas (30 sccm), and Ar gas (70 sccm) for 75 min.
5. Dry etch the Si by ICP-RIE with 100 W RF power, 0 W ICP power, 30 mTorr chamber pressure, and 40 sccm SF_6 gas for 6 min (**Figure 1o**).
6. To remove the PECVD oxide layer, dip the sample in BOE for 1 min 30 s, using a Teflon dipper.
7. Clean the sample sequentially with acetone, IPA, and DI water.
8. Deposit a SiO_2 layer with a thickness of 130 nm using PECVD with a temperature of 230 °C, 20 W RF power, 1000 mTorr pressure, SiH_4 gas (100 sccm), and N_2O gas (800 sccm) for 2 min.
9. Pattern the SiO_2 as a hard mask layer for dry etching.
    1. Spin coat positive PR on the sample at 4,000 rpm for 40 s and soft bake the coated sample at 90 °C for 90 s. Expose the sample to UV light with a photolithography mask for 10 s.
    2. Immerse the sample in the developer for 1 min to define the pattern, clean it in DI water, and dry it with an N_2 blowgun while holding it with forceps. Hard bake the sample for hardening the PR layer at 110 °C for 5 min.
    3. To pattern the SiO_2 hard mask, dip the sample in BOE for 1 min 30 s using a Teflon dipper, clean it in DI water, and dry it with an N_2 blowgun while holding it with forceps.

10. Dry etch the PI by RIE with 30 W RF power, O_2 gas (30 sccm), and Ar gas (70 sccm) for 75 min.
11. To remove the PECVD oxide layer, dip the sample in BOE for 30 s, using a Teflon dipper.

12. Clean the sample sequentially with acetone, IPA, and DI water. To remove the moisture, dry the clean sample with an N_2 blowgun while holding it with forceps.

6. Etching the Sacrificial Layer and Transferring the Sample to Flexible Substrate

NOTE: See **Figure 2**.

1. Etch the sacrificial layer by immersing the sample in hydrofluoric acid 49% for 20 min (**Figure 2a**; inset).
2. Rinse the sample with DI water.
3. After using the capillary phenomenon of a wiper to absorb the moisture between the substrate and the device, dry the clean sample with an N_2 blowgun while holding it with forceps to remove the remaining moisture (**Figure 2a**).
    1. Perform the process of rinsing and drying the sample. Due to the low adhesion between the device and the substrate, this has to be done very carefully, so as not to separate the substrate and the device.
4. Hold the sample using carbon tape and attach the water-soluble tape.
5. Strip off the water-soluble tape in an instant to prevent the device from remaining on the substrate (**Figure 2b**).
6. Confirm that the sample is attached to the water-soluble tape.
7. Transfer the sample to a polydimethylsiloxane (PDMS) coated polyethylene terephthalate (PET) film (**Figure 2c**).
    1. Prepare PDMS (10:1 mixture of prepolymer:curing agent) and remove any air bubbles in the PDMS by degassing.
    2. Spin coat the PDMS on the PET film at 1,000 rpm for 30 s and bake the PET film on a hot plate at a temperature of 110 °C for 10 min.
    3. Expose the sample to UV light for 30 s to improve the adhesion of the PDMS and attach the water-soluble tape with the sample to the PDMS-coated PET film.
    NOTE: UV treatment enhances the adhesion of a PDMS surface.
8. To remove the water-soluble tape, carefully drop water on it, using a pipette. Remove the water-soluble tape with a slow flow of water to prevent the device from being swept away by the water. Dry the sample slowly with an N_2 blowgun while holding it with forceps (**Figure 2d**).

Representative Results

Figure 3a and **3b** show the designed and fabricated structure of NIPIN PTR considering previous studies[2,23]. The inset in **Figure 3a** exhibits a basic I-V characteristic of PTR. The detailed structural parameters of PTR are shown in **Figure 3b**. The doping process for a Si layer on an SOI wafer was conducted using the ion implantation of the NNFC. The doping depth is ~1.25 μm, which is equal to the thickness of the Si layer, and the doping concentration of n^+ and p^+ are ~10^{19} cm^{-3}. The doping distribution on the top Si layer has a finger-type doping. The side depletion region between the n^+ region and p^+ region, which is generated by the finger-type doping, is useful to reduce the loss of photo-generated carriers[25]. Moreover, the finger-type doping broadens the active region generating photo-generated carriers, thereby increasing the cell efficiency. **Figure 3c** presents an optical image of doped Si PTR islands. The I-V characteristic of a single PTR is shown in **Figure 3d**.

Figure 4a displays the fabricated PTR array before a transfer printing step. A magnified image shows the single PTR cell in detail. The PI-encapsulated serpentine electrode provides stretchability to the device and protects the electrodes and Si cells from a crack or failure. In addition to mechanical stability, the PI layer plays a role as an antireflective coating by reducing the difference in refractive indices between the Si layer and air. **Figure 4b** shows the optical image for the transferred device onto a PDMS-coated PET film. By using a transfer printing method, the completed device can be placed on a flexible substrate (*e.g.*, a thin PET film). **Figure 4c** exhibits the schematic illustrations of the measurement setup and the definition of a radius of curvature (RoC). To measure an electrical performance in a bending state, we produced the custom-made manual stage to bend the sample by moving from side to side. **Figure 4d** shows the I-V characteristics of the PTR array in different RoCs (*i.e.*, infinity, 10 cm, 8 cm, 6 cm, 4 cm, 2 cm). This result demonstrates that the electrical feature of the PTR is constant, regardless of the RoCs. The light source used in this experiment is a white light induced by a halogen lamp. **Figure 4e** shows the ratio of the photocurrent to dark current as a function of voltage with different RoCs. The dynamic range, which determines the sensitivity of photodetector, is maintained at ~600 or more, above a bias voltage of 2 V. This result shows that a thin Si membrane can achieve a significant dynamic range due to a low dark current as shown in the inset of **Figure 4e**. **Figure 4f** displays the images for the bent PTR array with each RoC.

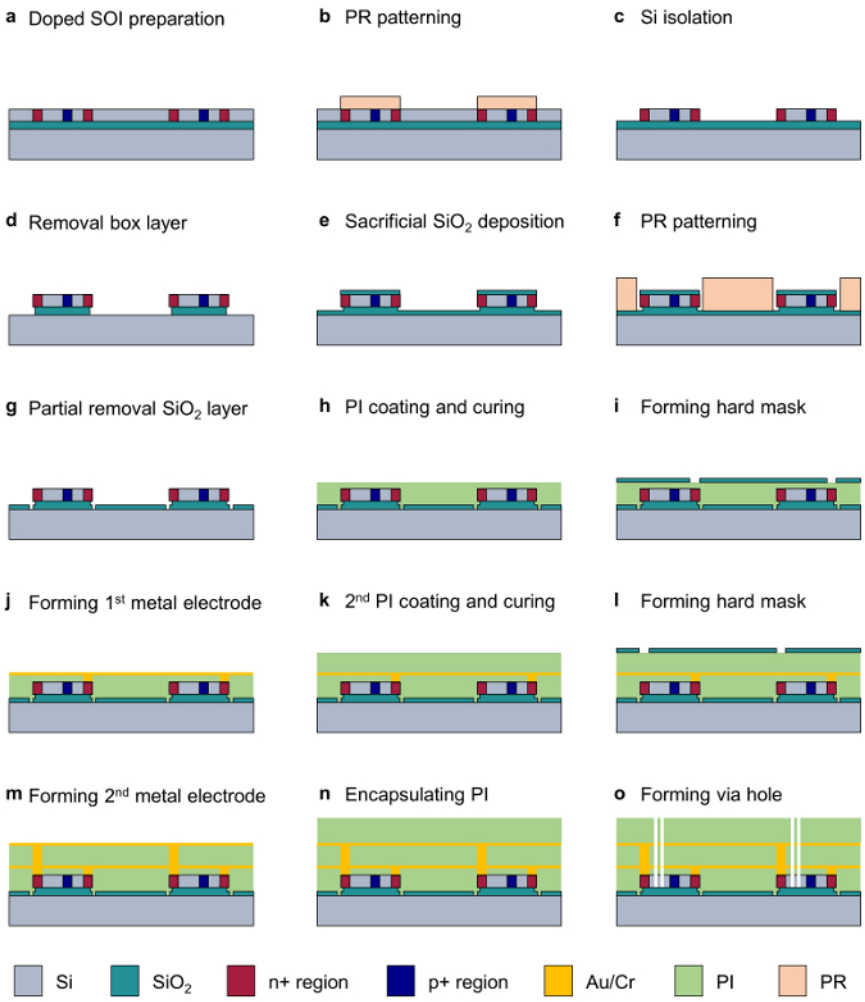

Figure 1: Schematic illustrations of the fabrication process of the curved phototransistor array. The panels (**a**) - (**o**) show the sequential process from fabricating a phototransistor device on a doped SOI substrate to creating a via hole to remove the sacrificial layer of the SOI substrate. Please click here to view a larger version of this figure.

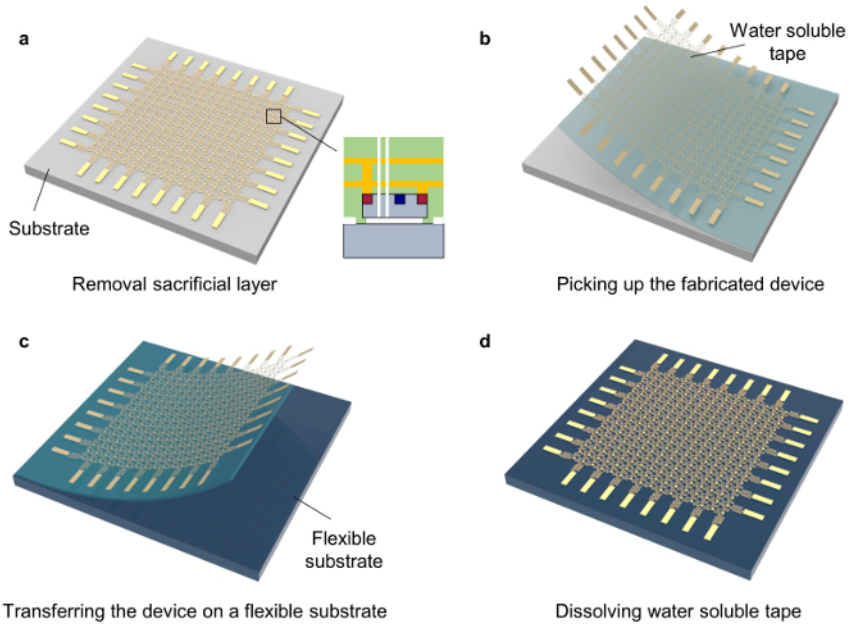

Figure 2: Schematic illustrations for the transfer printing of the phototransistor array from SOI wafer to flexible substrate. (**a**) This panel shows how to form an open mesh structure and remove the sacrificial layer. (**b**) This panel shows how to detach the device with water-soluble tape. (**c**) This panel shows how to transfer the device to a sticky flexible substrate (*e.g.*, PDMS). (**d**) This panel shows how to remove the water-soluble tape by dropping water on it. Please click here to view a larger version of this figure.

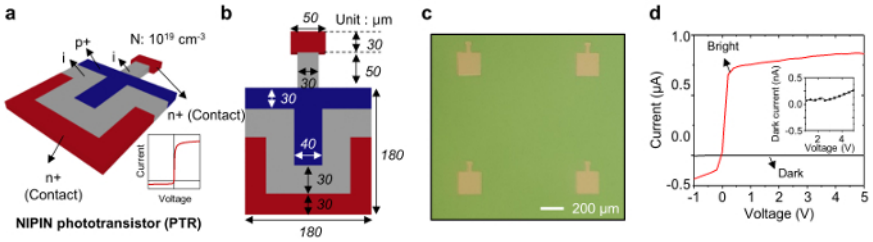

Figure 3: Schematics for the single unit cell of phototransistor (PTR) and simulation result of I-V characteristics. The first two panels show (**a**) a tilt view of the PTR and (**b**) a top view of the PTR. The doping concentration is ~10^{19} cm^{-3} for both of the p^+ and n^+ regions. The detailed geometrical values are displayed in **Figure 3b**. The inset in **Figure 3a** displays a basic I-V characteristic of the PTR. (**c**) This panel shows an optical microscopy image on doped Si PTRs. The yellow color indicates the Si PTRs. The green substrate is a SiO_2 box layer. (**d**) This panel shows the I-V characteristics of a single PTR under the bright and dark states. The inset shows the dark current of the single cell. Please click here to view a larger version of this figure.

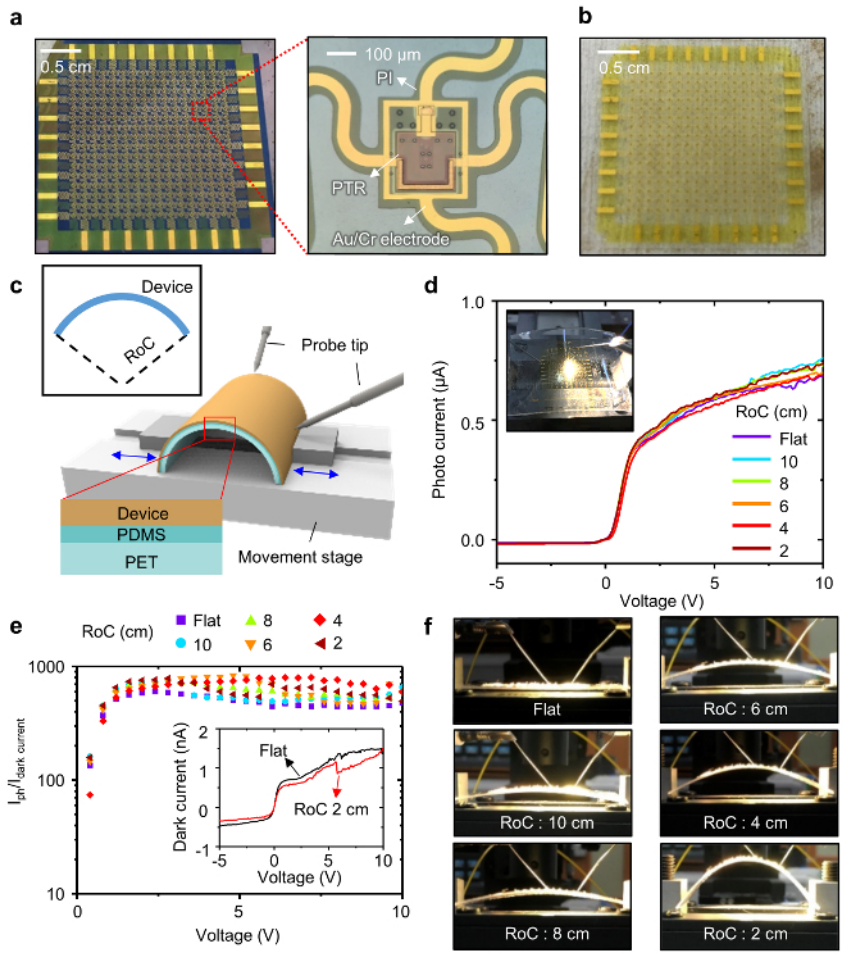

Figure 4: Schematic of methods and results for measuring I-V characteristics in the curved state of phototransistor array. (**a**) This panel shows the photography of the fabricated device. A magnified image shows the single PTR cell in detail. (**b**) This panel shows the photography of a transferred device on a PDMS-coated PET film. (**c**) This panel is a simplified schematic of the measurement setup. The radius of curvature (RoC) is defined as the radius of a circle from the center of the circle as illustrated in the inset. (**d**) This panel shows the I-V characteristics of the PTR array under illumination with different RoCs. (**e**) This panel is a plot of the ratio of the photocurrent to dark current. The inset demonstrates a very low dark current level, thereby causing a high dynamic range. (**f**) This panel shows optical images for the bent PTR array in each RoC. Please click here to view a larger version of this figure.

Discussion

The fabrication technology described here contributes significantly to the progress of advanced electronics and wearable devices. The fundamental concepts of this approach use a thin Si membrane and metal interconnectors capable of stretching. Although Si is a brittle and hard material that can easily be fractured, a very thin Si layer can obtain a flexibility[26,27]. In the case of the metal interconnector, the wavy shape offers stretchability and flexibility[28,29]. In particular, the metal interconnectors act as electrodes for the entire device to operate as a matrix type. The matrix form of an open mesh, which is implemented in the final step, provides softness to the device in a structured manner. Together with the merits of the thin Si layer and the serpentine electrodes, this achieves stress isolation and releases device geometry. Also, the PI layer that surrounds the whole device simultaneously offers the effects of antireflection and protects the device from cracks or defects. By using a transfer printing method, the fabricated device can be placed on a flexible substrate, and hence, it secures the condition that the device can be deformed. Through the process steps presented here, a Si device with many advantages in terms of device characteristics and process maturity can be realized as a deformable electronics.

To obtain a PTR cell with a low dark current, the device doping process is vital. The doping depth is more critical than the impurity concentration because the deep doping can form more depletion regions compared to that of shallow doping. In the depletion region, photo-generated electrons and holes do not recombine, and this is the primary factor reducing the dark current in deep-doped PTR. For deeper doping, an ion implantation method is more suitable than the diffusion method. We conducted the impurity doping by using the ion implantation method corresponding to step 1 in this protocol. To successfully execute the doping process, consider using commercial technology computer-aided design (TCAD) simulations to estimate the doping depth and concentration.

Metallization steps (step 3 and 4) are one of the most critical processes in the fabrication technology described here. In this protocol, Au is used as an electronic path, but Au has a poor adhesion with a PI layer. Thus, a Cr (or Ti) layer is necessary to promote the adhesion of Au and PI. Owing to PI thickness, which is ~1.2 μm in this experiment, metal lines deposited by an electron beam or thermal evaporations do not have a

sufficient step coverage. In this protocol, a sputtering process is used in this step. We recommend using a sputter process for the metallization. After the metal pattern is formed by solution etching, the sample is cleaned with DI water. A careful N_2 gas blow is then required to dry the water from the sample, because a strong gas blow may peel off the metal layers.

Forming a via hole (step 5), which penetrates both the PI and Si layers by an etching process, is also critical in this fabrication technology. It is difficult to decide whether the via hole patterns are well generated or not because the via holes have a small diameter (~2 μm). Since the color is changed after the etching process, we recommend observing the inside of the via hole patterns by microscope during each step. Then, the PI layer needs to be patterned in the form of a serpentine mesh. This is an essential step for the device to obtain a flexible/stretchable property.

For the removal of the sacrificial SiO_2 layer (step 6), it is essential to know the etching degree of the box oxide layer by hydrofluoric acid (HF) through continuous microscopic observation. Also, drying DI water that has remained after cleaning the HF should be carefully executed, because blowing the N_2 gas may peel off the device from the handling Si substrate. We recommend blowing the N_2 gas gently. Because HF is very harmful to the human body, the experiment should be conducted in an environment equipped with protective gear, protective gloves, and a gas venting system. The subsequent step in this protocol, the transfer printing process (step 6), needs fastidious and skilled techniques. For instance, when removing the device using a water-soluble tape, it is advantageous to secure the yield by removing the tape at a high speed.

In conclusion, this article presented a process for fabricating a flexible Si PTR array using a series of semiconductor fabrication processes such as a deposition, etching, photolithography, and transfer printing. For the insight of this fabrication process, this article illustrated specific fabrication methods with detailed descriptions. Also, this article described how we used the approach described here to fabricate the sample and measure the device performance of the fabricated samples in I-V characteristics with and without the illumination for different RoCs. This result demonstrates that the Si PTR array has a mechanical and electrical stability in a deformed state. In this study, the mechanical limitations of the Si materials are overcome by introducing a structure capable of a three-dimensional deformation into Si, which is not inherently soft. Because of this, the fabrication procedure can also be useful for other applications in the field of flexible/stretchable electronics and wearable devices such as healthcare monitors.

Disclosures

The authors have nothing to disclose.

Acknowledgements

This research was supported by the Creative Materials Discovery Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT (NRF-2017M3D1A1039288). Also, this research was supported by the Institute for Information and Communications Technology Promotion (IITP) grant funded by the Korea government (MSIP) (No.2017000709, Integrated approaches of physically unclonable cryptographic primitives using random lasers and optoelectronics).

References

1. Ko, H. C. *et al.* A hemispherical electronic eye camera based on compressible silicon optoelectronics. *Nature.* **454**, 748-753 (2008).
2. Song, Y. M. *et al.* Digital cameras with designs inspired by the arthropod eye. *Nature.* **497** (7447), 95-99 (2013).
3. Jung, I. *et al.* Dynamically tunable hemispherical electronic eye camera system with adjustable zoom capability. *Proceedings of the National Academy of Sciences of the United States of America.* **108** (5), 1788-1793 (2011).
4. Floreano, D. *et al.* Miniature curved artificial compound eyes. *Proceedings of the National Academy of Sciences of the United States of America.* **110** (23), 9267-72 (2013).
5. Liu, H., Huang, Y., Jiang, H. Artificial eye for scotopic vision with bioinspired all-optical photosensitivity enhancer. *Proceedings of the National Academy of Sciences of the United States of America.* **113** (23), 3982-3985 (2016).
6. Pang, K., Fang, F., Song, L., Zhang, Y., Zhang, H. Bionic compound eye for 3D motion detection using an optical freeform surface. *Journal of the Optical Society of America B.* **34** (5), B28-B35 (2017).
7. Lee, G. J., Nam, W. I., Song, Y. M. Robustness of an artificially tailored fisheye imaging system with a curvilinear image surface. *Optics & Laser Technology.* **96**, 50-57 (2017).
8. Xu, X., Mihnev, M., Taylor, A., Forrest, S. R. Organic photodetector arrays with indium tin oxide electrodes patterned using directly transferred metal masks. *Applied Physics Letters.* **94** (4), 1-3 (2009).
9. Deng, W. *et al.* Aligned single -crystalline perovskite microwire arrays for high -performance flexible image sensors with long -term stability. *Advanced Materials.* **18** (11), 2201-2208 (2016).
10. Liu, X., Lee, E. K., Kim, D. Y., Yu, H., Oh, J. H. Flexible organic phototransistor array with enhanced responsivity via metal-ligand charge transfer. *ACS Applied Materials & Interfaces.* ***8*** .(11), 7291-7299 (2016).
11. Li, X. *et al.* Constructing fast carrier tracks into flexible perovskite photodetectors to greatly improve responsivity. *ACS Nano.* **11** (2), 2015-2023 (2017).
12. Li, L., Gu, L., Lou, Z., Fan, Z., Shen, G. ZnO quantum dot decorated Zn_2SnO_4 nanowire heterojunction photodetectors with drastic performance enhancement and flexible ultraviolet image sensors. *ACS Nano.* **11** (4), 4067-4076 (2017).
13. Dumas, D. *et al.* Infrared camera based on a curved retina. *Optics Letters.* **37** (4), 653-655 (2012).
14. Dumas, D., Fendler, M., Baier, N., Primot, J., le Coarer, E. Curved focal plane detector array for wide field cameras. *Applied Optics.* **51** (22), 5419-5424 (2012).
15. Gregory, J. A. *et al.* Development and application of spherically curved charge-coupled device imagers. *Applied Optics.* **54** (10), 3072-3082 (2015).
16. Guenter, B. *et al.* Highly curved image sensors: a practical approach for improved optical performance. *Optics Express.* **25** (12), 13010-13023 (2017).

17. Wu, T. *et al.* Design and fabrication of silicon-tessellated structures for monocentric imagers. *Microsystems & Nanoengineering.* **2**, 16019 (2016).
18. Yoon, J. *et al.* Flexible concentrator photovoltaics based on microscale silicon solar cells embedded in luminescent waveguides. *Nature Communications.* **2**, 343 (2011).
19. Lee, S. M. *et al.* Printable nanostructured silicon solar cells for high-performance, large-area flexible photovoltaics. *ACS Nano.* **8** (10), 10507-10516 (2014).
20. Kang, D. *et al.* Flexible opto-fluidic fluorescence sensors based on heterogeneously integrated micro-VCSELs and silicon photodiodes. *ACS Photonics.* **3** (6), 912-918. (2016).
21. Van den Brand, J. *et al.* Flexible and stretchable electronics for wearable health devices. *Solid-State Electronics.* **113**, 116-120. (2015).
22. Yu, K. J. *et al.* Bioresorbable silicon electronics for transient spatiotemporal mapping of electrical activity from the cerebral cortex. *Nature Materials.* **15**, 782-791. (2015).
23. Kim, M. S., Lee, G. J., Kim, H. M., Song, Y. M. Parametric optimization of lateral NIPIN phototransistors for flexible image sensors. *Sensors.* **17** (8), 1774 (2017).
24. Kim, D. H., *et al.* Stretchable and foldable silicon integrated circuits. *Science.* **320**, 507-511 (2008).
25. Shin, K. S., *et al.* Characterization of an integrated fluorescence-detection hybrid device with photodiode and organic light-emitting diode. *IEEE Electron Device Letters.* **27** (9), 746-748. (2006).
26. Lu, N. Mechanics, materials, and functionalities of biointegrated electronics. *The Bridge.* **43** (4), 31-38 (2013).
27. Burghartz, J. N. *et al.* Ultra-thin chip technology and applications, a new paradigm in silicon technology. *Solid-State Electronics.* **54** (9), 818-829 (2010).
28. Shin, G. *et al.* Micromechanics and advanced designs for curved photodetector arrays in hemispherical electronic-eye cameras. *Small.* **6** (7), 851-856 (2010).
29. Jung, I. *et al.* Paraboloid electronic eye cameras using deformable arrays of photodetectors in hexagonal mesh layouts. *Applied Physics Letters.* **96** (2), 21110 (2010).

